Crystal Image through Imaging Innovation

PIXELPLUS

PX6130KA

1/3.75” 1.3MP RGB Bayer / YUV CMOS Image Sensor one chip

120dB HDR 30 fps

Preliminary specification

Ver 0.1

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General Description

The PX6130KA is the 1/3.75” CMOS image sensor (CIS) one chip integrated with ISP function blocks designed to support 1.3MP at 30 frames per second (fps). The device is fully AEC-Q100 (Grade 2) qualified with a -40°C to 105°C wide temperature range. The chip is designed according to ISO26262 ASIL-B requirement. The PX6130KA employs a number of safety mechanisms that can be enabled to detect and inform any errors from the sensor.

The PX6130KA consists of 1336 (H) x 1016 (V) effective pixels with 20 pixels on each side for optical center adjustment and 8 pixels on each side for color interpolation. The image sensor present these features like as motion free high dynamic range (HDR) to 120 dB. It enables the PX6130KA shows no saturation image in the worst contrast situations.

The PX6130KA has excellent noise performance for low light condition and high dynamic range (HDR) support using by DCG (Dual Conversion Gain) and multi- exposure method up to 120dB. It incorporates on-chip ISP functions such as Lens Shade Correction (LSC), Defective Pixel Correction (DPC), Purple Fringing Reduction (PFR), Block Level Compensation (BLC), HDR Combine, Tonemap, Demosaic, Denoise, Dehaze, Gamma Correction, Color Correction Matrix, Edge Enhancement, Color Enhancement, Auto Exposure, Auto White Balance and so on.

The PX6130KA is suitable for a surround-view camera and a rear view camera with 2.8V/1.8V/1.2V power supply.

Applications

- Surround View Monitoring System (SVM)
- Rear View Camera
- E-Mirror

Features

- Support for display image size 1280 x 960 with 1.3MP
- Provide for effective image size 1336 x 1016 for mechanical alignment adjustment +40(H), +40(V) and for color processing +16(H), +16(V)
- Support for high dynamic range 120dB with DCG (Dual Conversion Gain) and multi exposure method
- Implemented ASIL-B safety function
- Qualified to AEC-Q100 (Grade 2)
- Support for combined RGB bayer / YUV output format : DVP 12bit RAW and 8bit YUV / MIPI 2-lanes RAW / YUV
- Support for image signal processing functions such as LSC, DPC, PFR, BLC, HDR Combine, Tonemap, Demosaic, Denoise, Dehaze, Gamma Correction, Color Correction Matrix, Edge enhancement, Color Enhancement, AE, AWB, etc
- Programmable frame size, window size, and exposure
- Support for external synchronization capability (Genlock)
- Built-in 2K bit of one-time programmable memory (OTP) for storing the chip information and chip calibration
- Embedded temperature sensor for monitoring junction temperature of CIS
- Embedded spread spectrum clock generation (SSCG) for EMI avoidance
- Available Anti-Reflection (AR) coating Glass

Key Performance Parameter

Parameter	Typical value
Pixel size	3.0 um x 3.0 um
Effective pixel array	1336(H) x 1016(V)
Effective image area	4.008 mm x 3.048 mm
Optical format	1/3.75 inch
Input clock frequency	27 [MHz]
Output interface	2-Lane MIPI / DVP Combo with RAW / YUV data
Max. frame rate	HDR 30 fps
Dark signal	TBD e/sec
Sensitivity	TBD V/Lux·s
Power supply	HVDD : 1.8~2.8 [V] AVDD : 2.8 [V] DVDD : 1.2 [V]
Power consumption	TBD
Operating temp.	-40~105 [°C] (Ambient)
Max. dynamic range	120 dB
SNR	TBD [dB]
Package type	A-CSP
Package size	5.945mm x 5.945mm x 0.876mm

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1. Application system

1.1. System overview

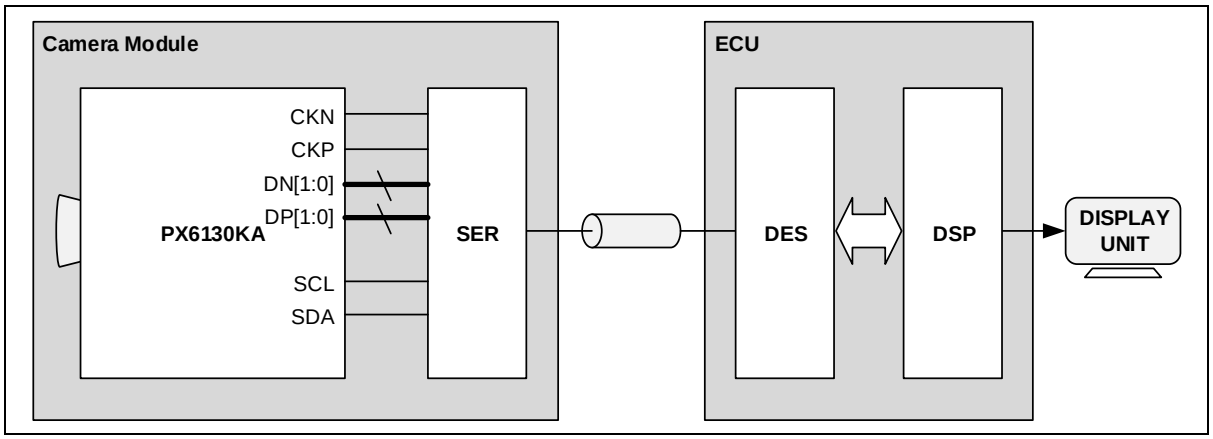
The PX6130KA one chip has a 1/3.75” optical format, 1280 x 960 display array, 3.0um DCG pixel and HDR sensor intended for low-cost SVM/RVC applications for the automotive market.

The PX6130KA has the function of output 12-bit compression mapped HDR combined image using the 2- exposure with DCG. The device generates the 3-image capture for acquiring 120dB HDR image. It supports output interfaces such as 2-lane MIPI and 12-bit DVP.

1.1.1. Standalone camera

Figure 1 shows the block diagram of the standalone camera application. Through the LVDS SERializer and DESerializer (SERDES), the video stream data is transmitted over a long distance from the camera module to the electronic control unit (ECU).

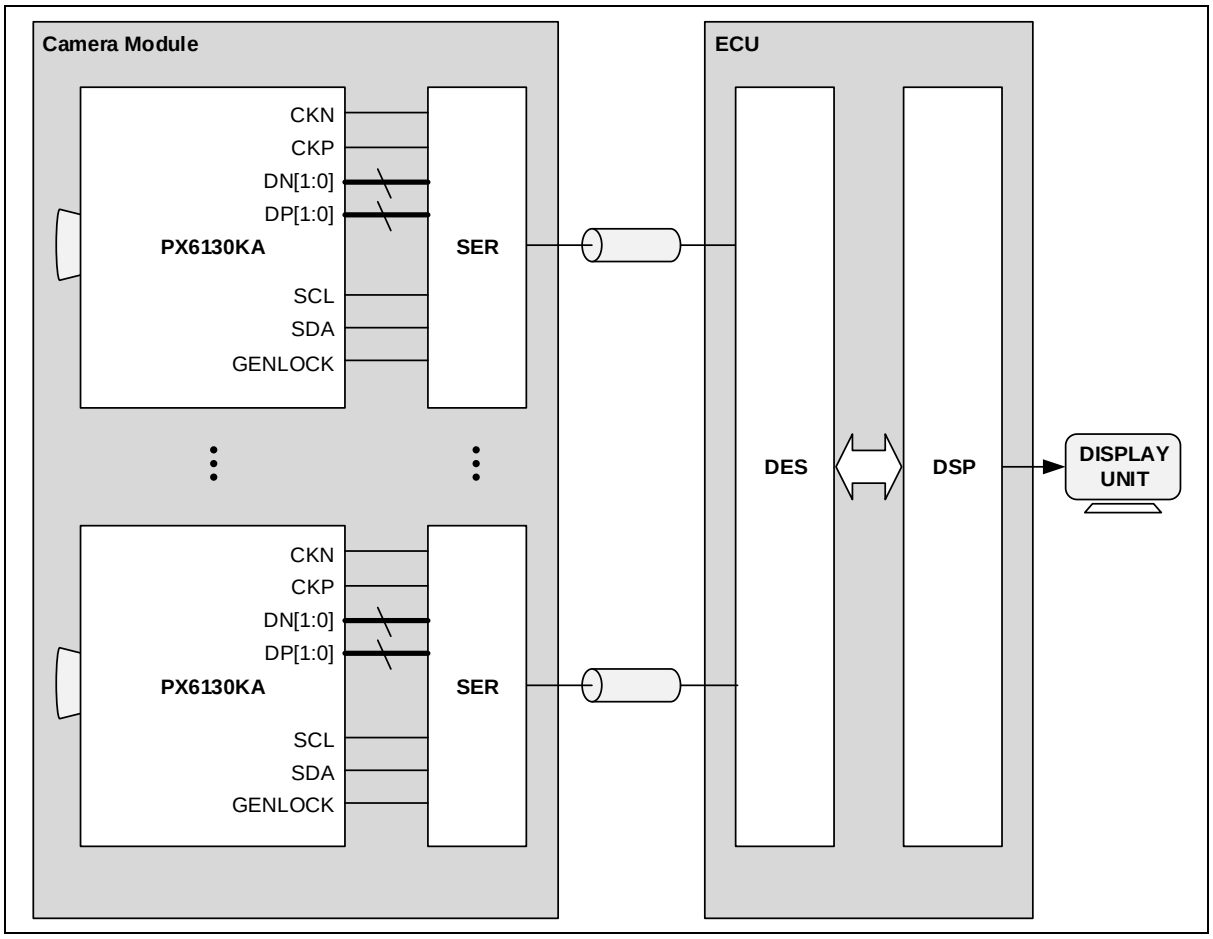
Figure 1. Standalone camera block diagram for automotive applications



1.1.2. Multi-camera system

Figure 2 shows a block diagram of a typical multi-camera application in which the video streaming signal from several sensor modules can be synchronized together at the back channel through programming sensor registers by the ECU.

Figure 2. Multi-camera block diagram



1.2. Ball configuration and assignment (64-Ball)

Figure 3. A-CSP Ball Map(Bottom View)

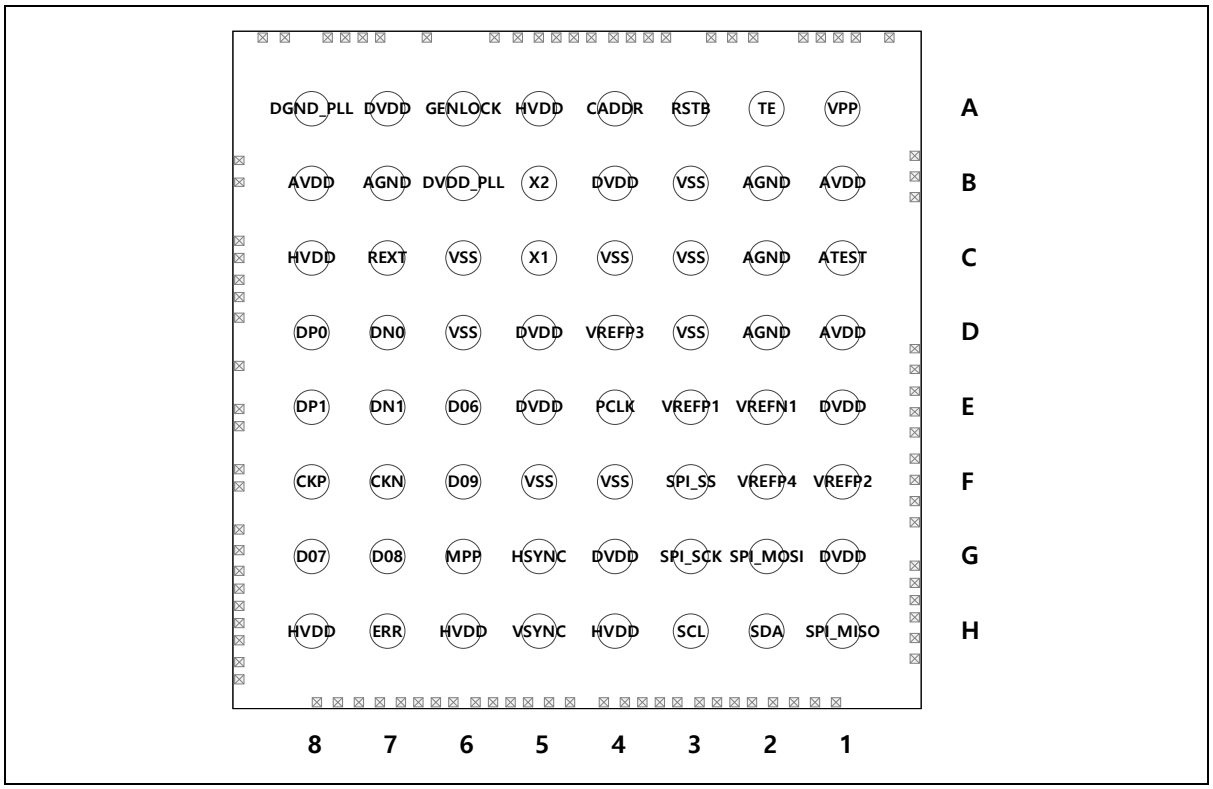


Table 1. Ball Descriptions

Ball	Ball Name	IO	Pull up/ Pull down	Ball Description
A1	VPP	O	-	OTP programing Voltage output
A2	TE	I	-	Chip test enable
A3	RSTB	I	-	System reset must remain low for at least 8 master clocks after power is stabilized. When the chip is reset, all registers are set to their default values.
A4	CADDR	I	-	I2C slave device address selection pin. Multi-purpose pin function is supported. When Multi-purpose pin function mode is enabled, I2C slave device address selection pin is tied to GND internally. (ERR (Alarm)/UART Rx/PWM3/GPIO[9])
A5	HVDD	P	-	IO VDD 1.8V ~ 2.8V DC It should be tied with nearby HGND by 1uF bypass capacitors.
A6	GENLOCK	BIO	-	External Frame sync input. Slave chip can receive the external frame sync signal from master chip/External Frame sync output. Master chip can output the external frame sync signal through this pad to synchronize all digital outputs of two or more chips. Multi-purpose pin function is supported. (ERR (Alarm)/UART Rx/PWM2/GPIO[8])
A7	DVDD	P	-	Digital (Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
A8	DGND_PLL	P	-	PLL GND

Ball	Ball Name	IO	Pull up/ Pull down	Ball Description
B1	AVDD	P	-	Analog VDD 2.8V It should be tied with nearby AGND by both 1uF bypass capacitors.
B2	AGND	P	-	Analog GND
B3	VSS	P	-	Digital(Core) GND
B4	DVDD	P	-	Digital (Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
B5	X2	O	-	Master clock input pad (Crystal output)
B6	DVDD_PLL	P	-	Digital (Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
B7	AGND	P	-	Analog GND
B8	AVDD	P	-	Analog VDD 2.8V It should be tied with nearby AGND by both 1uF bypass capacitors.
C1	ATEST	O	-	Analog test output
C2	AGND	P	-	Analog GND
C3	VSS	P	-	Digital(Core) GND
C4	VSS	P	-	Digital(Core) GND
C5	X1	I	-	Master clock input pad
C6	VSS	P	-	Digital(Core) GND
C7	REXT	O	-	External Resistor for MIPI
C8	HVDD	P	-	IO VDD 1.8V ~ 2.8V DC It should be tied with nearby HGND by 1uF bypass capacitors.
D1	AVDD	P	-	Analog VDD 2.8V It should be tied with nearby AGND by both 1uF bypass capacitors.
D2	AGND	P	-	Analog GND
D3	VSS	P	-	Digital(Core) GND
D4	VREFP3	O	-	VREFP3 output. It should be tied with nearby AGND by 1uF bypass capacitors.
D5	DVDD	P	-	Digital (Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
D6	VSS	P	-	Digital(Core) GND
D7	DN0/D1	O	-	MIPI DN0 Output / Digital Output bit 1
D8	DP0/D0	O	-	MIPI DP0 Output / Digital Output bit 0
E1	DVDD	P	-	Digital (Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
E2	VREFN1	O	-	VREFN1 output. It should be tied with nearby AGND by 1uF bypass capacitors.
E3	VREFP1	O	-	VREFP1 output. It should be tied with nearby AGND by 1uF bypass capacitors.
E4	PCLK	O	-	Digital Output Data can be latched by external devices at the rising or falling edge of PCLK

Ball	Ball Name	IO	Pull up/ Pull down	Ball Description
E5	DVDD	P	-	Digital (Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
E6	D6	O	-	Digital Output bit 6. Multi-purpose pin function is supported. (ERR (Alarm)/UART Rx/PWM2/GPIO[2])
E7	DN1/D3	O	-	MIPI DN1 Output / Digital Output bit 3
E8	DP1/D2	O	-	MIPI DP1 Output / Digital Output bit 2
F1	VREFP2	O	-	VREFP2 output. It should be tied with nearby AGND by 1uF bypass capacitors.
F2	VREFP4	O	-	VREFP4 output. It should be tied with nearby AGND by 1uF bypass capacitors.
F3	SPI_SS	O	-	Serial Peripheral Interface - Slave Select
F4	VSS	P	-	Digital(Core) GND
F5	VSS	P	-	Digital(Core) GND
F6	D9	O	-	Digital Output bit 9. Multi-purpose pin function is supported. (ERR (Alarm)/JTAG TMS/UART Tx/PWM1/GPIO[5])
F7	CKN/D5	O	-	MIPI Clock Negative Output / Digital Output bit 5
F8	CKP/D4	O	-	MIPI Clock Positive Output / Digital Output bit 4
G1	DVDD	P	-	Digital (Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
G2	SPI_MOSI	BIO	-	Serial Peripheral Interface - Master Output, Slave Input
G3	SPI_SCK	O	-	Serial Peripheral Interface - Serial Clock
G4	DVDD	P	-	Digital(Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
G5	HSYNC	O	-	Horizontal synchronization pulse. HSYNC is high (or low) for the horizontal window of interest. It can be programmed to appear or not outside the vertical window of interest. Multi-purpose pin function is supported. (ERR (Alarm)/JTAG TCK/UART Tx/PWM3/GPIO[7])
G6	MPP	BIO	-	Multi-purpose Pin Function Output (Digital Video Out(D11)/ERR (Alarm)/JTAG_TRSTn/UART Tx/PWM1/GPIO[1])
G7	D8	O	-	Digital Output bit 8. Multi-purpose pin function is supported. (ERR (Alarm)/JTAG TDO/UART Rx/PWM0/GPIO[4])
G8	D7	O	-	Digital Output bit 7. Multi-purpose pin function is supported. (ERR (Alarm)/UART Tx/PWM3/GPIO[3])
H1	SPI_MISO	BIO	-	Serial Peripheral Interface - Master Input, Slave Output
H2	SDA	BIO	-	2-wire serial interface clock, SDA line is pulled up to HVDD by off-chip resistor
H3	SCL	I	-	2-wire serial interface data, SCL line is pulled up to HVDD by off-chip resistor
H4	HVDD	P	-	IO VDD 1.8V ~ 2.8V DC It should be tied with nearby VSS by 1uF bypass capacitors.
H5	VSYNC	O	-	Vertical sync : Indicates the start of a new frame. Multi-purpose pin function is supported. (ERR (Alarm)/JTAG TDI/UART Rx/PWM2/GPIO[6])

Ball	Ball Name	IO	Pull up/ Pull down	Ball Description
H6	HVDD	P	-	IO VDD 1.8V ~ 2.8V DC It should be tied with nearby VSS by 1uF bypass capacitors.
H7	ERR	BIO	-	Safety error output. When a safety error occurs, '1' is output. Multi-purpose pin function is supported. (Digital Video Out(D10)/ERR (Alarm)/UART Tx/PWM0/GPIO[0])
H8	HVDD	P	-	IO VDD 1.8V ~ 2.8V DC It should be tied with nearby VSS by 1uF bypass capacitors.

1.3. Reference Schematic

Figure 4 shows the reference schematic with power supply and signal connection of the PX6130KA. The PX6130KA chip is powered from AVDD, DVDD, HVDD. The range of each power sources is as follows.

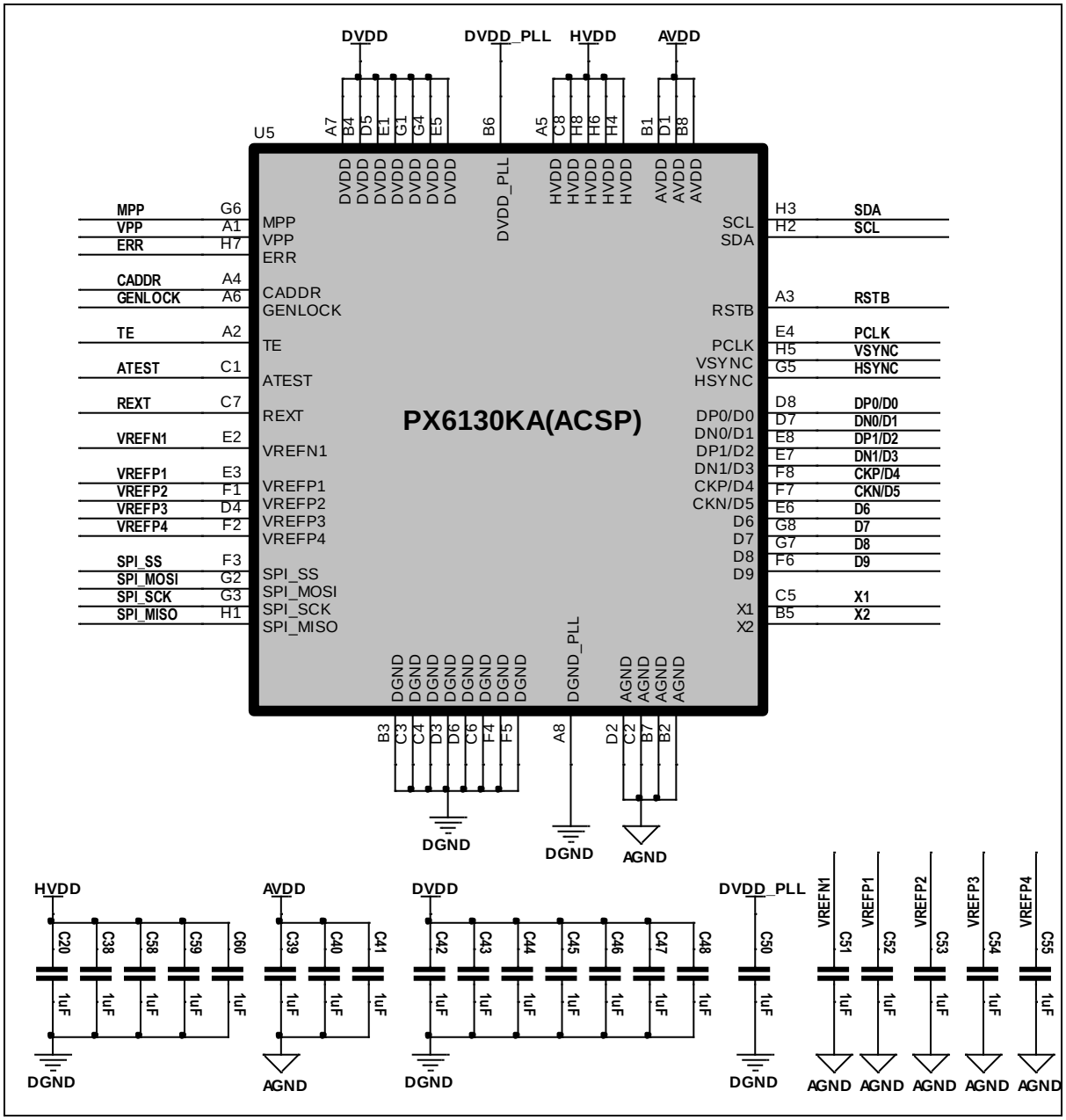
Analog power supply AVDD: 2.8V

Digital power supply DVDD: 1.2V

I/O power supply HVDD: 1.8V/2.8V.

(Figure 4 reference schematic is preliminary data)

Figure 4. PX6130KA (A-CSP) reference schematic



1.4. Power Sequence

When starting the PX6130KA chip, it is best to apply all external applied power at the same time, otherwise DVDD must be applied first and then another power shall be applied. Reset must be maintained for 8 clock (X1) after HVDD is applied and then turned off.

Figure 5. PX6130KA Power Sequence

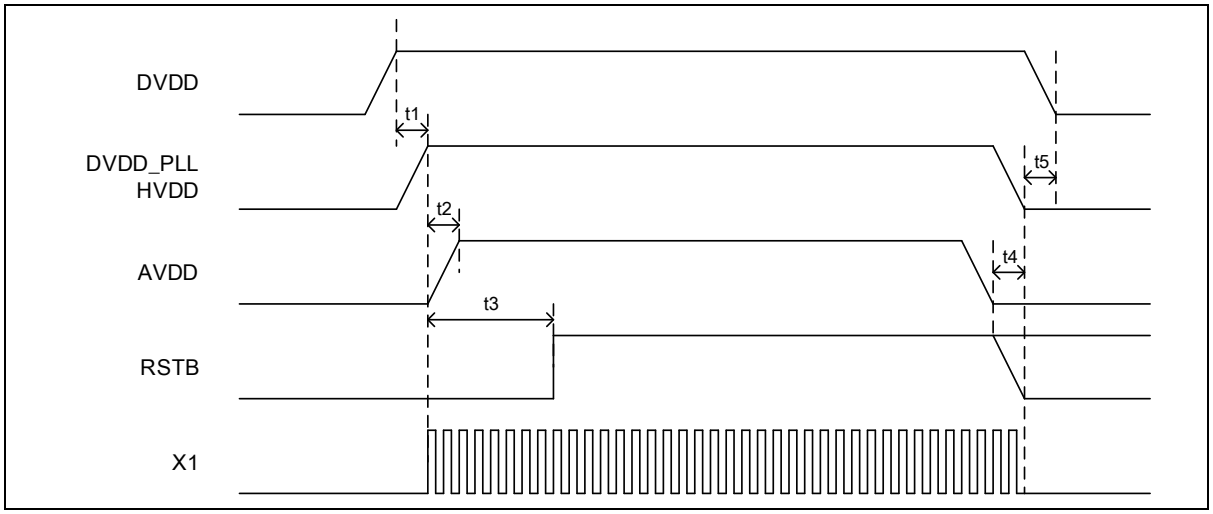


Table 2. Power sequence timing constraint

Symbol	Description	Min	Max	Unit
t1	From DVDD rising to HVDD, DVDD_PLL rising	0	10	ms
t2	From HVDD, DVDD_PLL rising to AVDD	0	10	ms
t3	period of maintaining the reset after DVDD rising	8		X1
t4	From AVDD falling to HVDD, DVDD_PLL falling	0		ms
t5	From HVDD, DVDD_PLL falling to DVDD falling	0		ms

1.5. System Reset

For initialization, PX6130KA requires reset fed from the RSTB pin. The RSTB is asynchronous LOW active input. The width of reset pulse should be above 1 cycle of main clock (27MHz). The reset pulse is clocked by main clock and regenerated within PX6130KA.

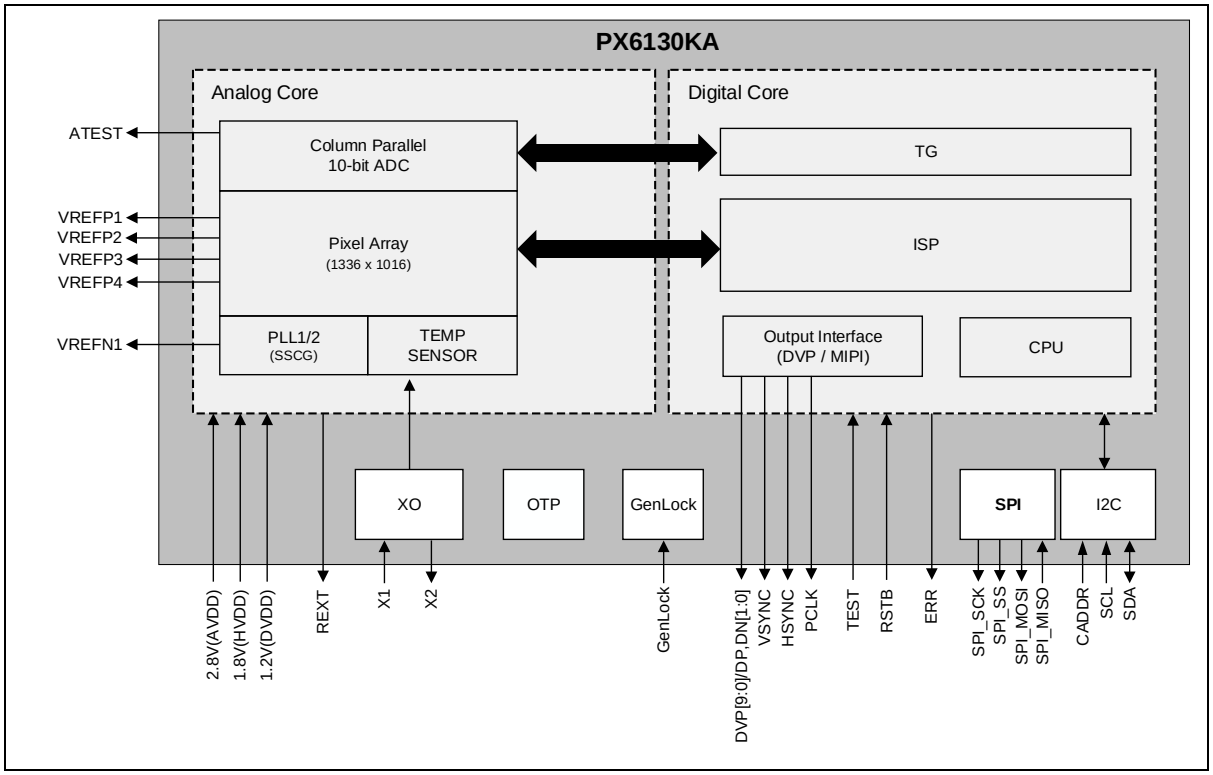
Table 3. Register Table – Soft reset

Address	Register Name	R/W	Update	Init Value	Description	
0xF000_0030	Soft_reset	R/W	AT	32’hFFFF_FFFF	[31] :	Software Reset All (0 : Reset enable, 1 : Normal)
					[11] :	MIPI Tx Reset (0 : Reset enable, 1 : Normal)
					[10] :	VOUT_X2 Reset (0 : Reset enable, 1 : Normal)
					[9] :	ISP/TG Reset (0 : Reset enable, 1 : Normal)
					[8] :	MCLK Reset (0 : Reset enable, 1 : Normal)
					[7] :	GPIO Reset (0 : Reset enable, 1 : Normal)
					[6] :	UART Reset (0 : Reset enable, 1 : Normal)
					[5] :	WDT Reset (0 : Reset enable, 1 : Normal)
					[4] :	TIMER Reset (0 : Reset enable, 1 : Normal)
					[3] :	QSPI Reset (0 : Reset enable, 1 : Normal)
					[2] :	APB Reset (0 : Reset enable, 1 : Normal)
					[1] :	AXI Reset (0 : Reset enable, 1 : Normal)
					[0] :	CPU Reset (0 : Reset enable, 1 : Normal)

2. Chip Architecture

Figure 6 shows the top level block diagram of the PX6130KA.

Figure 6. Chip Architecture



The PX6130KA is supported to provide a fully ISP processed YUV output. It integrates a high performance ISP blocks with HDR function to obtain high quality images. The processed YUV is output from a DVP/MIPI interface.

The PX6130KA consists of two functional blocks: Analog Core and Digital Core block.

The Analog Core consists of pixel array, Analog to Digital Converter (ADC), temperature sensor, One Time Programmable memory (OTP), and MIPI transmitter block. The pixel array are composed of photodiodes and generate electron-hole pairs in proportion to the intensity of incoming light. The generated electron-hole pairs are converted into a voltage using a combination of charge pump and row driver and are transferred to ADC, the voltage is converted into a digital value by applying Correlation Dual Sampling (CDS) operation in ADC and ramp signal blocks, and its digital output value is transferred to digital core block.

The Digital Core consists of Timing Generation (TG), Image Signal Processing (ISP), Formatter and OTP controller blocks. The TG generates a signal for controlling the analog circuit of the Analog Core and receives a 3-image digital value (2-exposure mode & DCG) from the Analog Core. The 3-image value is transferred to the ISP after processing the Black Level Compensation (BLC).

The ISP consists of Lens Shade Correction (LSC), Defective Pixel Correction (DPC), Purple Fringing Reduction (PFR), Block Level Compensation (BLC), HDR Combine, Tonemap, Demosaic, Denoise, Dehaze, Gamma Correction, Color Correction Matrix (CCM), Edge Enhancement, Color Enhancement, Auto Exposure (AE), Auto White Balance (AWB) and so on. The processed RAW or YUV data is delivered to the formatter.

The Formatter changes the output data to the desired format such as RAW / YUV data through DVP and MIPI interfaces.

The OTP controller may store or read data in the OTP. The OTP controller stores measured data in OTP for correct calculation of defective pixel correction (DPC) and temperature sensors. It then reads the data stored in OTP and forwards it to the DPC or temperature sensor.

The PX6130KA supports Dual Conversion Gain (DCG) HDR image and extra very short image with separate exposure time so that three images are acquired to generate 120dB HDR images. The brightness of the acquired image varies depending on the time of exposure to light.

The DCG can use either high conversion gain (HCG) or low conversion gain (LCG). The LCG is used for high bright intensity and HCG is used for low bright intensity. In a bright environment, it can less detect light using LCG and can further express images of bright areas. In a dark environment, it can further detect light using HCG and further express images of dark areas.

Table 4 show the operation modes supported for HDR.

Table 4. HDR operation mode

Operation mode		DCG	Exposure
3HDR	L (Long)	HCG	1-exposure
	S (Short)	LCG	1-exposure
	VS (Very Short)	HCG/LCG	2-exposure

The PX6130KA also supports the generator lock (genlock) function that synchronizes the internal synchronous timing to the external input frame sync. The PX6130KA supports output interfaces such as 2-lane MIPI and 12-bit DVP.

Table 5 show the operating modes supported and maximum possible frame rates in each mode.

Table 5. Operating mode

No.	Operation mode	Image Structure	Interface	Bit Width	Max. Frmae rate [fps]
1	2-exposure with DCG	1280x960	DVP	12-bit	30
2		1280x960	MIPI	12-bit	30

3. Analog Core

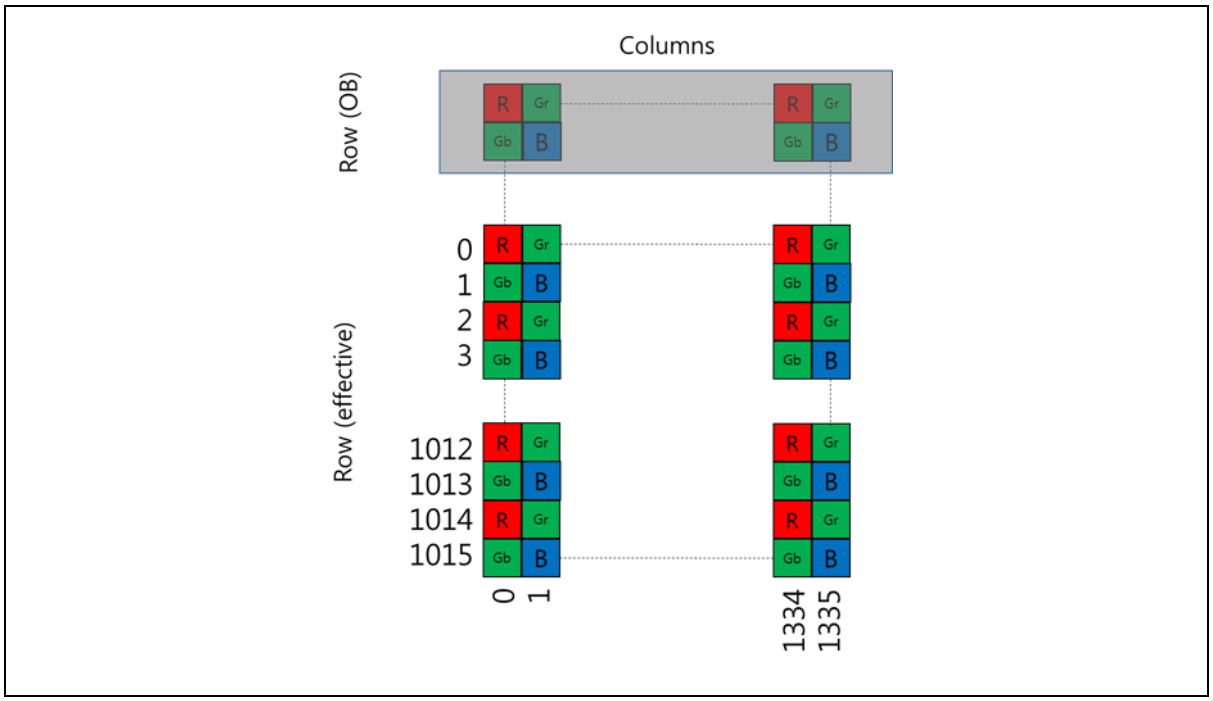
3.1. Pixel Array Structure

The PX6130KA sensor has a total effective image array of 1336 columns by 1016 rows (including display image arrays of 1280x960) covered by color filters Bayer(R, Gr, Gb and B) pattern. Figure 7 shows the pixel array color filter layout. In addition to the effective pixel, Optical block (OB) pixels area embedded to serve as reference pixels for the black level compensation (BLC). The OB Pixels are covered with a metal layer light shield.

The entire readable column is 1320 active column + 8 active border columns (interpolation pixel) + 8 dummy active border columns = 1336 columns

The entire readable row is 1000 active column + 8 active border rows (interpolation pixel) + 8 dummy active border rows = 1016 rows

Figure 7. pixel array structure



3.2. Frame Structure

The frame consists of Row Optical Black Pixel (ROBP) region, Effective Pixel, Crop Window, and Window. ROBP region is an area that does not receive light, and Effective Pixel is an area that receives light. The value of the effective pixel is adjusted based on the ROBP value, and the function is Black Level Compensation (BLC). Crop window determines the input image size for reading pixel data from the Effective Pixel. Window determines the size of the output image. (refer to Figure 8)

The size of the frame is adjustable by "framewidth" and frameheight and must be larger than ROBP region and crop window. (refer to Figure 8, Figure 9)

Pixel scanning is performed row by row on entire frame. Frame row counter and frame column counter, which are limited by “framewidth” and frameheight values respectively, are used to indicate the current coordinate of pixel being scanning. The column counter value increases by every pixel clock (pclk). Every time the column counter reaches maximum value, the row counter is increase. Origin point (0, 0) of row and column counter value is in the top left corner of each frame.

The maximum size of Crop window is 1336x1016 pixels. The user cannot change Crop window on the x-axis but can change Crop window in 2-pixel units based on the start and end points on the y-axis. If offsets of start and end point are same, Crop window satisfy image center regardless of vertical mirror. frameheight determines “fheight_a”, “rjump_top”, and “rjump_bot”. (refer to Figure 8,Table 6)

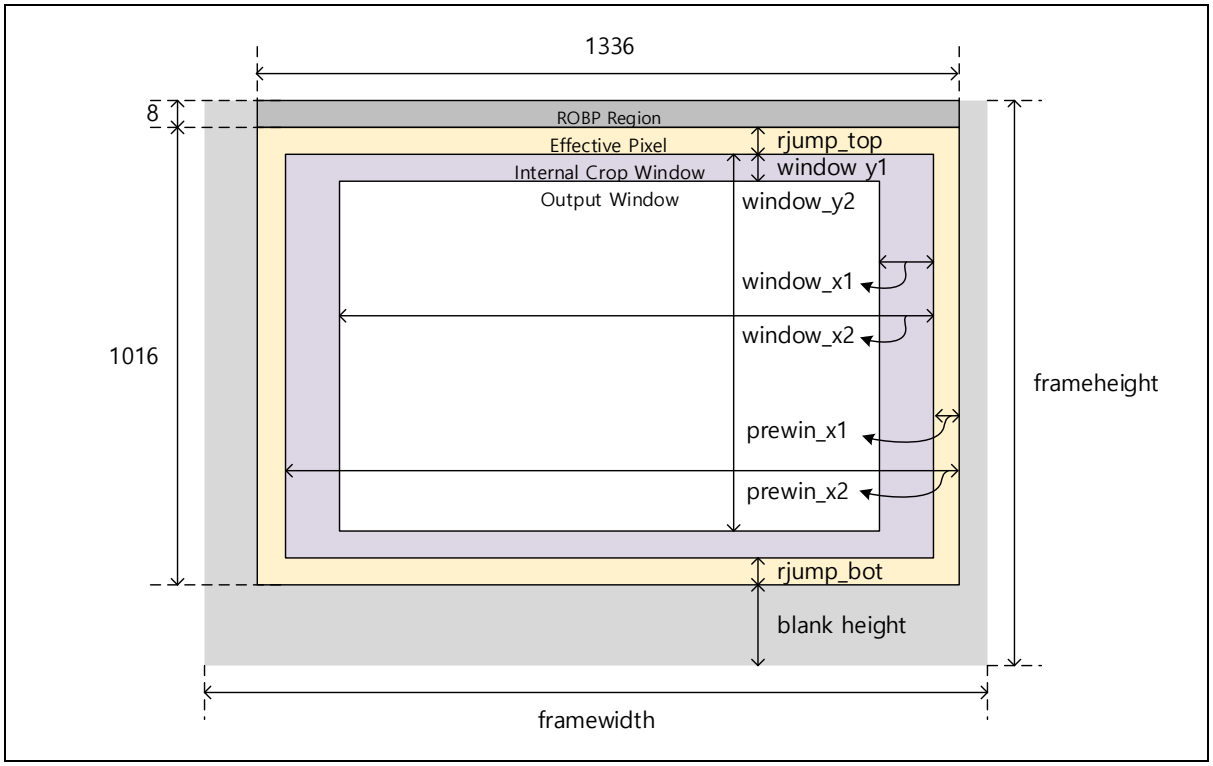
➔ frameheight = “fheigtht_a” – (“rjump_top” + “rjump_bot”)

The size of Crop window is adjusted to "rjump_top" and "rjump_bot". As the value of the "rjump_top" register increases, the starting point of Crop window increases. As the value of the "rjump_bot" register increases, the end point of Crop window decreases. (refer to Figure 8)

The maximum size of Window is determined by Crop window and is 1336x1016 pixels. The x-axis and y-axis can be changed in 2-pixel units to prevent bayer pattern order from reversing. (refer to Figure 8)

The size of Window is adjusted to "window_x1", "window_x2", "window_y1" and "window_y2". As the "window_x1" register value increases, the starting point of Window increases on the x-axis. As the "window"x2" register value increases, the end point of Window increases on the x-axis. As the value of the "window_y1" register increases, the starting point of Window increases on the y-axis. As the value of the "window_y2" register increases, the end point of Window increases on the y-axis. (refer to Figure 8)

Figure 8. Frame structure



If registers are default values, the frame structure behaves as shown below.(refer to Figure 9)

Figure 9. Default frame structure

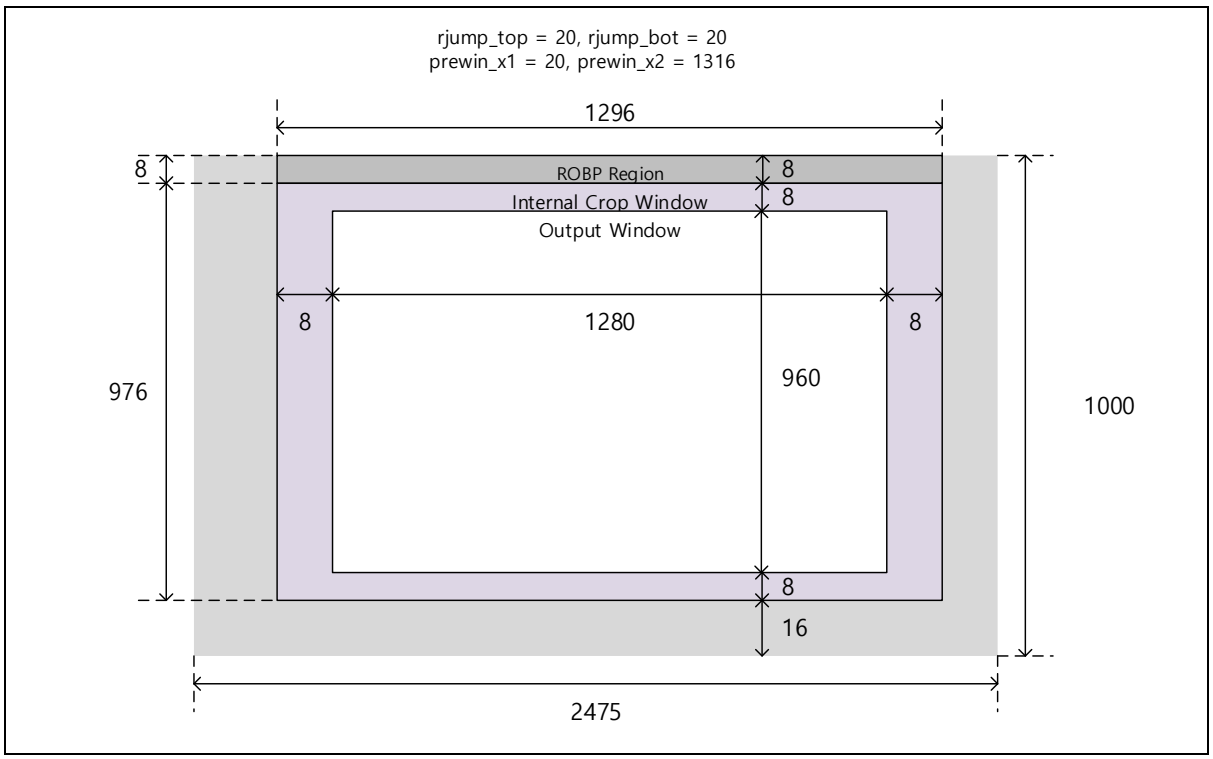
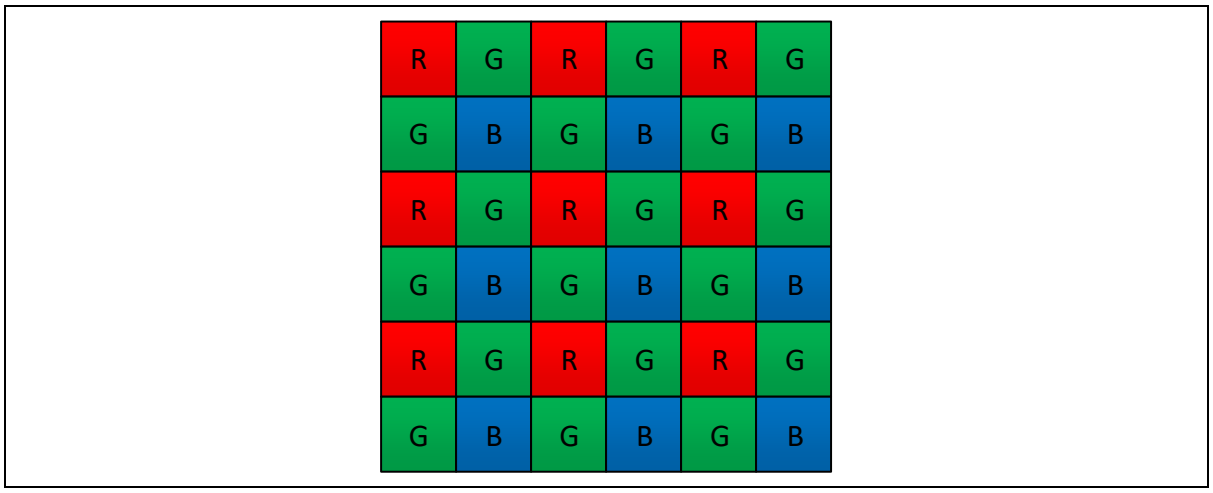


Table 6. Register Table - Frame structure

Address	Register Name	R/W	Update	Init Value	Description	
0xF070_0010	framewidth	R/W	AT	13’h9AA	[12:8] :	Framewidth High Byte (must be larger than window width)
					[7:0] :	Framewidth Low Byte (must be larger than window width)
0xF070_0014	fheight	R/W	AT	13’h3E7	[12:8] :	Frameheight High Byte (must be larger than window height)
					[7:0] :	Frameheight Low Byte (must be larger than window height)
0xF060_4010	prewin_x1	RW	AT	11’h14	[26:16]	Internal horizontal cropping start point
	prewin_x2			11’h524	[10:0]	Internal horizontal cropping end point
0xF071_006C	rjump_top	R/W	AT	13’h014	[12:8]	Row jump top value High Byte
					[7:0] :	Row jump top value Low Byte
0xF071_0070	rjump_bot	R/W	AT	13’h014	[12:8]	Row jump bottom value High Byte
					[7:0] :	Row jump bottom value Low Byte
0xF064_1010	wndow_x1	RW	AT	11’h008	[26:16]	Output horizontal cropping start point
	wndow_x2			11’h508	[10:0]	Output horizontal cropping end point
0xF064_1014	window_y1	RW	AT	11’h008	[26:16]	Output vertical cropping start point
	window_y2			11’h3C8	[10:0]	Output vertical cropping end point

3.3. Pixel Data Format

Figure 10. Bayer color filter pattern data



The pixel array is covered by bayer color filters as shown in the Figure 10. Since each pixel can have only one type of filter on it, only one-color component can be produced by a pixel. PX6130KA provides RGB bayer pattern data through a 10-bit channel which passes one-pixel data to the output bus at every pclk.

The PX6130KA provides horizontal, vertical mirror which respectively reverse the sensor data readout order horizontally and vertically. The user can change “mirror” to change readout order. (refer to Table 7)

Figure 11 Mirror shows a normal image and a mirrored image.

Figure 11. Mirror

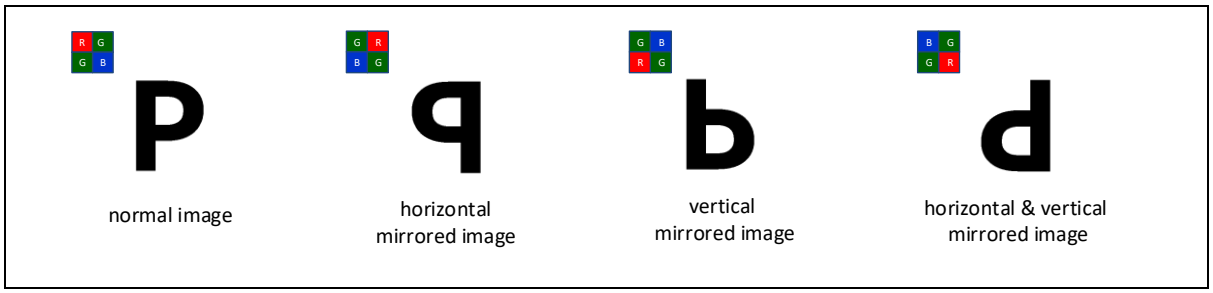


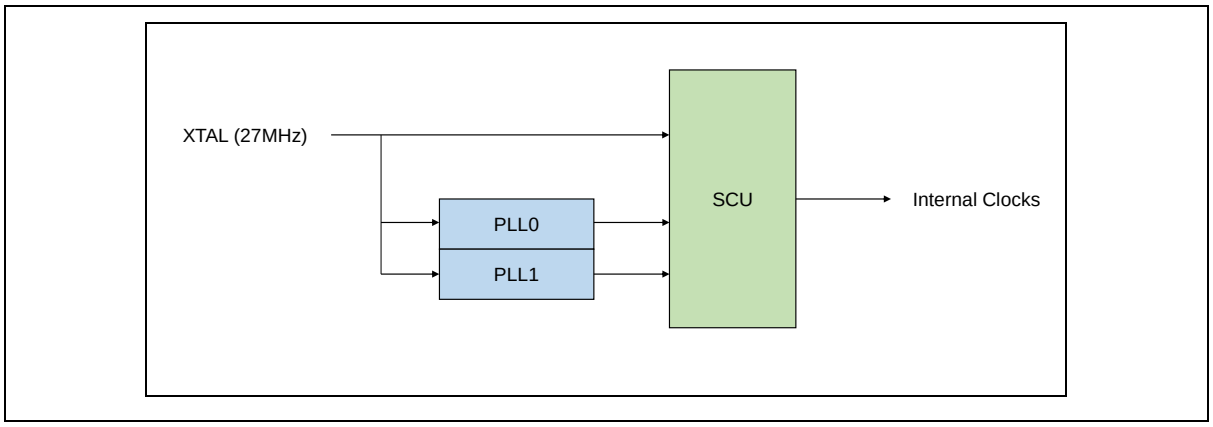
Table 7. Register Table - Mirror

Address	Register Name	R/W	Update	Init Value	Description
0xF070_016C	mirror	R/W	AT	2’h0	[1:0] : Image Inversion mirror [1]: vertical inversion mirror [0]: horizontal inversion

3.4. Clock

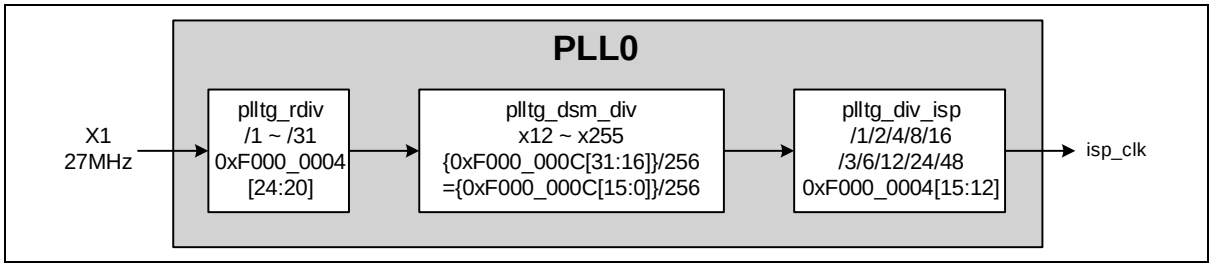
For the clock fed at internal processing blocks, PX6130KA includes two PLL. One is used to generate clocks for CPU, Bus and ISP block. The other is used to support MIPI Tx clocks. To generate various operating clocks properly, two MPLL should be set correctly depending on sensor frame structure. The reference clock is 27MHz, which is fed from crystal oscillator pad (X1, X2). The SCU (System Control Unit) in PX6130KA provides various clocks selectively to each functional block as figure below. Changing clock frequency, disabling unused clocks for reducing power dissipation also can be supported by setting the SCU.

Figure 12. Clock Generation and Control Schemetic



3.4.1. PLL

Figure 13. PLL0 Diagram



To overcome the EMI issue, spread spectrum clocking (SSC) is supported in this PLL0 to distribute the power on the ISP clock signal. Spread profile is a triangular shape. The spectrum can be up-spread, center-spread, or down-spread depending on the f_{SSC_UPPER} and f_{SSC_LOWER} frequency setting. $f_{SSC\_MOD\_RATE}$ is the modulation frequency, which is normally designed to be 30 kHz~33 kHz in many designs. f_{SSC_DEV} is modulation amplitude, which is smaller than 5000 ppm. SSC parameters calculation are given by following equations:

$$f_{SSC\_UPPER} = f_{REF} / plltg\_rdiv * plltg\_dsm\_div\_upper * (1 / plltg\_div\_isp)$$

$$f_{SSC\_LOWER} = f_{REF} / plltg\_rdiv * plltg\_dsm\_div\_lower * (1 / plltg\_div\_isp)$$

$$plltg\_dsm\_ystep = 256*(plltg\_dsm\_div\_upper – plltg\_dsm\_div\_lower)/8$$

$$plltg\_dsm\_xstep = f_{REF}/ plltg\_rdiv * 1/(2*f_{SSC\_MOD\_RATE}) * (1/ plltg\_dsm\_ystep)$$

The PLL1 generates clock for MIPI. The VCO range is from 445MHz to 594MHz. A programmable clock is provided to generate different frequencies.

Figure 14. PLL1 Diagram

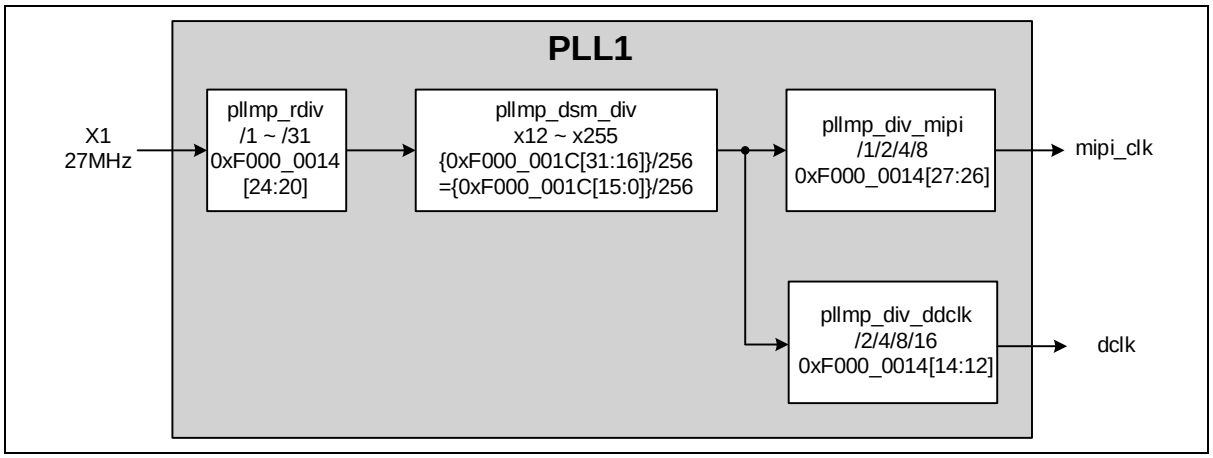


Table 8. Register Table – PLL

Address	Register Name	R/W	Update	Init Value	Description	
0xF000_0000	Mpll0_config0				[31:1]	Reserved
		RW	AT	1’b1	[0]	PLLTG_PD
0xF000_0004	Mpll0_config1	RW	AT	2’b01	[31:30]	plltg_ctrl_icp
				2’b10	[29:28]	plltg_div_cntr
				2’b10	[27:26]	plltg_div_ramp
				1’b0	[25]	plltg_dsm_clk_sel
				5’h01	[24:20]	plltg_rdiv
				2’b01	[19:18]	plltg_ioffset
				1’b0	[17]	plltg_ioffset_en
				1’b0	[16]	plltg_cp_dc_amp_sel
				4’b0011	[15:12]	plltg_div_isp
				2’b11	[11:10]	plltg_vco_band
				2’b00	[9:8]	plltg_dsm_dither
				2’b00	[7:6]	plltg_dsm_dtamp
				2’b10	[5:4]	plltg_vhigh_ctrl
				2’b10	[3:2]	plltg_vlow_ctrl
				1’b1	[1]	plltg_bypass_en
				1’b1	[0]	plltg_ana_lock_detect_pd
0xF000_0008	Mpll0_config2	RW	AT	2’b10	[29:28]	plltg_c1_sel
				4’b1100	[27:24]	plltg_c2_sel
				5’b00101	[20:16]	plltg_r2_sel
				8’h00	[15:8]	plltg_dsm_xstep

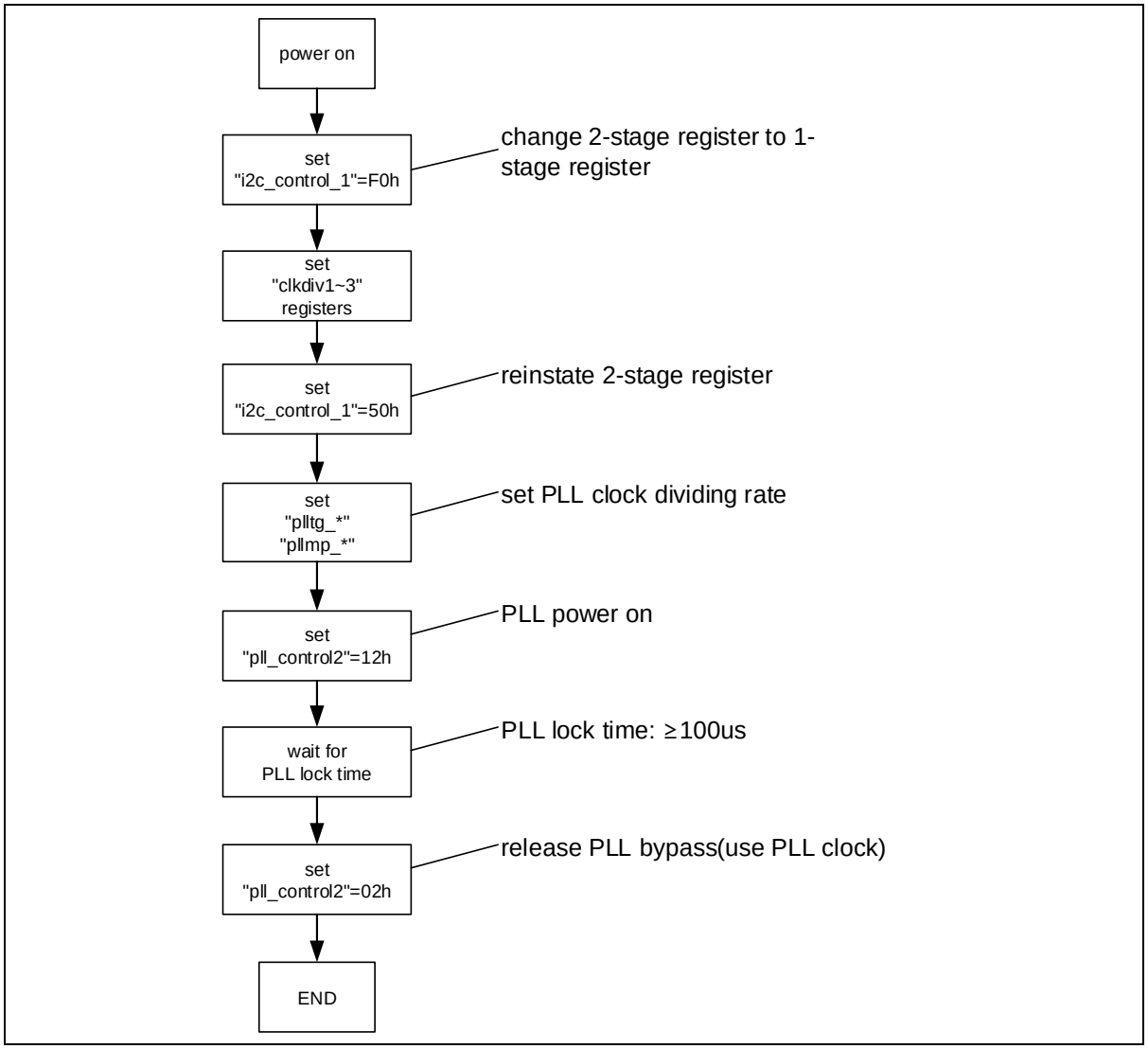
Address	Register Name	R/W	Update	Init Value	Description	
				8’h00	[7: 0]	plltg_dsm_ystep
0xF000_000C	Mpll0_config3	RW	AT	16’h1600	[31:16]	plltg_dsm_divh
				16’h1600	[15:0]	plltg_dsm_divl
0xF000_000C	Mpll0_config3	RW	AT	16’h1600	[31:16]	plltg_dsm_divh
0xF000_0010	Mpll0_config0	RW	AT		[31:1]	Reserved
				1’b1	[0]	PLLTG_PD
0xF000_0014	Mpll0_config1	RW	AT	2’b01	[31:30]	pllmp_ctrl_icp
				2’b10	[29:28]	pllmp_div_cntr
				2’b10	[27:26]	pllmp_div_ramp
				1’b0	[25]	pllmp_dsm_clk_sel
				5’h01	[24:20]	pllmp_rdiv
				2’b01	[19:18]	pllmp_ioffset
				1’b0	[17]	pllmp_ioffset_en
				1’b0	[16]	pllmp_cp_dc_amp_sel
				4’b0011	[15:12]	pllmp_div_isp
				2’b11	[11:10]	pllmp_vco_band
				2’b00	[9:8]	pllmp_dsm_dither
				2’b00	[7:6]	pllmp_dsm_dtamp
				2’b10	[5:4]	pllmp_vhigh_ctrl
				2’b10	[3:2]	pllmp_vlow_ctrl
				1’b1	[1]	pllmp_bypass_en
				1’b1	[0]	pllmp_ana_lock_detect_pd
0xF000_0018	Mpll0_config2	RW	AT	2’b10	[29:28]	pllmp_c1_sel
				4’b1100	[27:24]	pllmp_c2_sel
				5’b00101	[20:16]	pllmp_r2_sel
				8’h00	[15:8]	pllmp_dsm_xstep
				8’h00	[7: 0]	pllmp_dsm_ystep
0xF000_001C	Mpll0_config3	RW	AT	16’h1600	[31:16]	pllmp_dsm_divh
				16’h1600	[15:0]	pllmp_dsm_divl

3.4.2. PLL and Clock Setting Sequence

When using PLL, set-up sequence, show Figure 15, is necessary.

I2C update timing register, “i2c_control_1”, is changed before setting clock dividers to immediately apply clock divider settings.

Figure 15. Clock setting sequence



3.5. Temperature sensor

The PX6130KA has an embedded temperature sensor to measure its die junction temperature. The temperature can be read 9-bit through “temperature_h [0]” and “temperature_l [7:0]” registers. The “temperature_h” stores the sign part and the “temperature_l” stores the integer part of the value, all in degrees Celsius. If temperature is under 0°C, “temperature_h” is set to 0x01, if temperature is over 0°C, “temperature_h” is set to 0x00. The “temperature_l” takes value from 0x00 to 0xFF, which are corresponding to a valid readout temperature range from -40°C to 125°C.

The temperature sensor accuracy is ±2°C from -40°C to 125°C. The temperature data is being updated at every frame or every “ts_interval”, when register “ts_en” is high.

Table 9 shows the table of code-temperature conversion.

Table 9. Code-Temperature conversion table

Register Value		Temperature value [°C]
temperature_h[0] [bin]	temperature_l[7:0] [hex]	
1’b1	0x28	-40°C
1’b1	0x27	-39°C
…	…	…
1’b1	0x01	-1°C
1’b0	0x00	0°C
1’b0	0x01	1°C
…	…	…
1’b0	0x31	49°C
1’b0	0x32	50°C
1’b0	0x33	51°C
…	…	…
1’b0	0x7C	124°C
1’b0	0x7D	125°C

Table 10. Register Table – temperature sensor setting

Address	Register Name	R/W	Update	Init Value		Description
0xF070_0084	ts_ctrl0	RW	AT		[32:8]	reserved
				1’b0	[7]	Temperature sensor enable
				1’b0	[6]	Temp Sensor Mode 1’b0 : normal / 1’b1 : VCTAT triming
				2’b01	[5:4]	Tempe Sensor CLK div 1/32,1/64,1/128,1/256
				4’b0100	[3:0]	Tempe Sensor BGR VCTAT
0xF070_0088	ts_ctrl1	RW	AT		[32:8]	reserved
				1’b0	[7]	Temperature sensor OTP read mode
				1’b1	[6]	Temperature sensor BGR power down
				1’b1	[5]	Temperature sensor BGR clk bypass
				3’b011	[4:2]	Temperature sensor BGR chopper clock div (pclk/2^n)
				1’b0	[1]	Temperature sensor Test enable

Address	Register Name	R/W	Update	Init Value	Description
				1’h1	[0] Temperature sensor power down

4. Digital core

The Digital Core consists of Timing Generator (TG), Image Signal Processing (ISP), Formatter, CPU and OTP controllers. This chapter describes TG, ISP, Formatter and CPU. For OTP controllers, see the chapter OTP memory.

4.1. Timing Generator

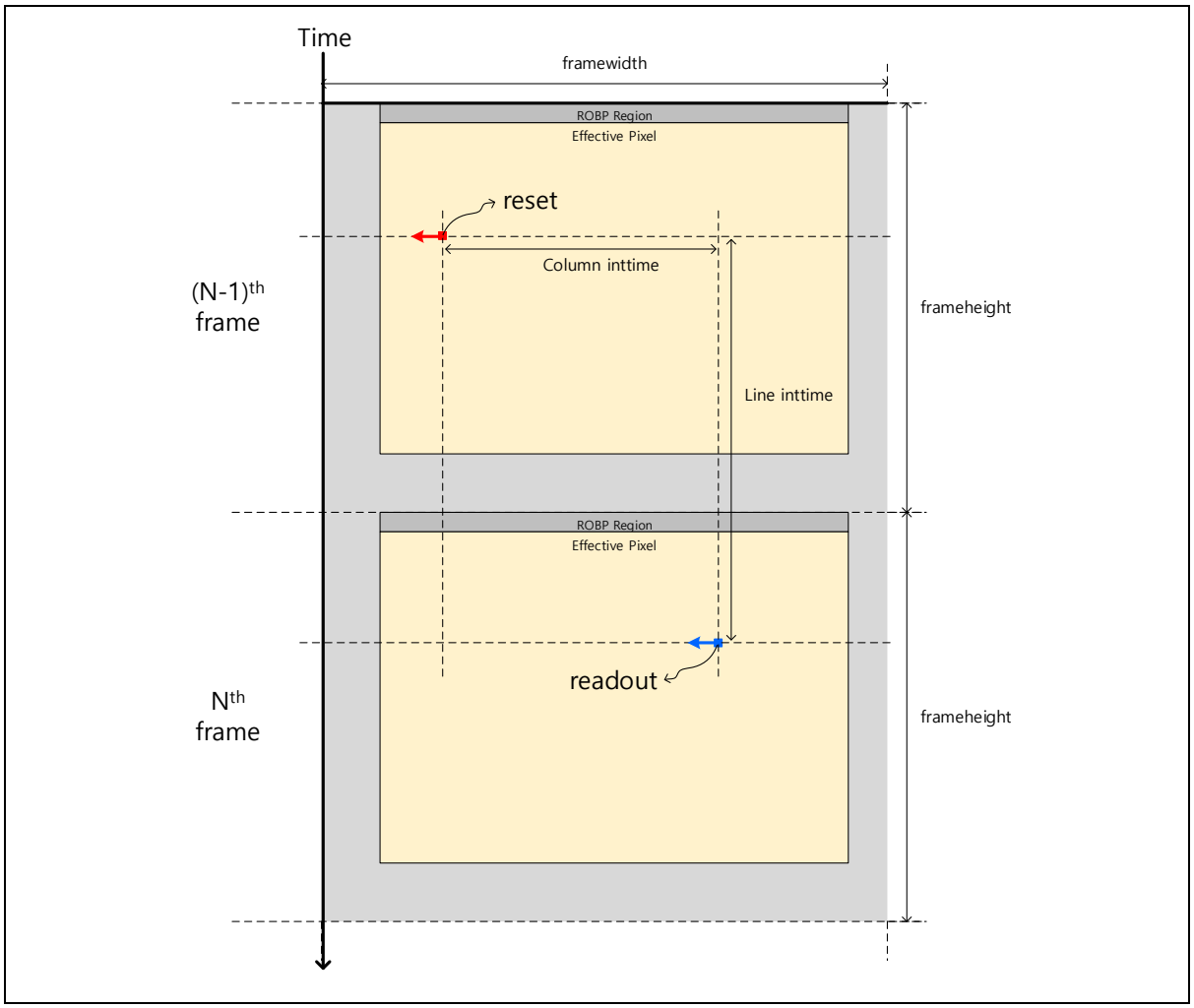
The TG generates signals that control analog circuits in the image sensor core, and can control exposure time and global gain. The data received from the image sensor core is processed with functions such as Black Level Calibration (BLC), Digital Gain, and White Balance Gain. And the data can be replaced with test pattern data. It has a Genlock function that synchronizes data timing with the master device.

4.1.1. Exposure Control

The PX6130KA may adjust the brightness of an image by integration time, gain, and digital gain.

4.1.1.1. Integration Time

Figure 16. Integration time structure in PX6130KA



PX6130KA employs rolling shutter for capturing image. Rolling shutter operate read process after reset process in row sequence. (refer to Figure 16)

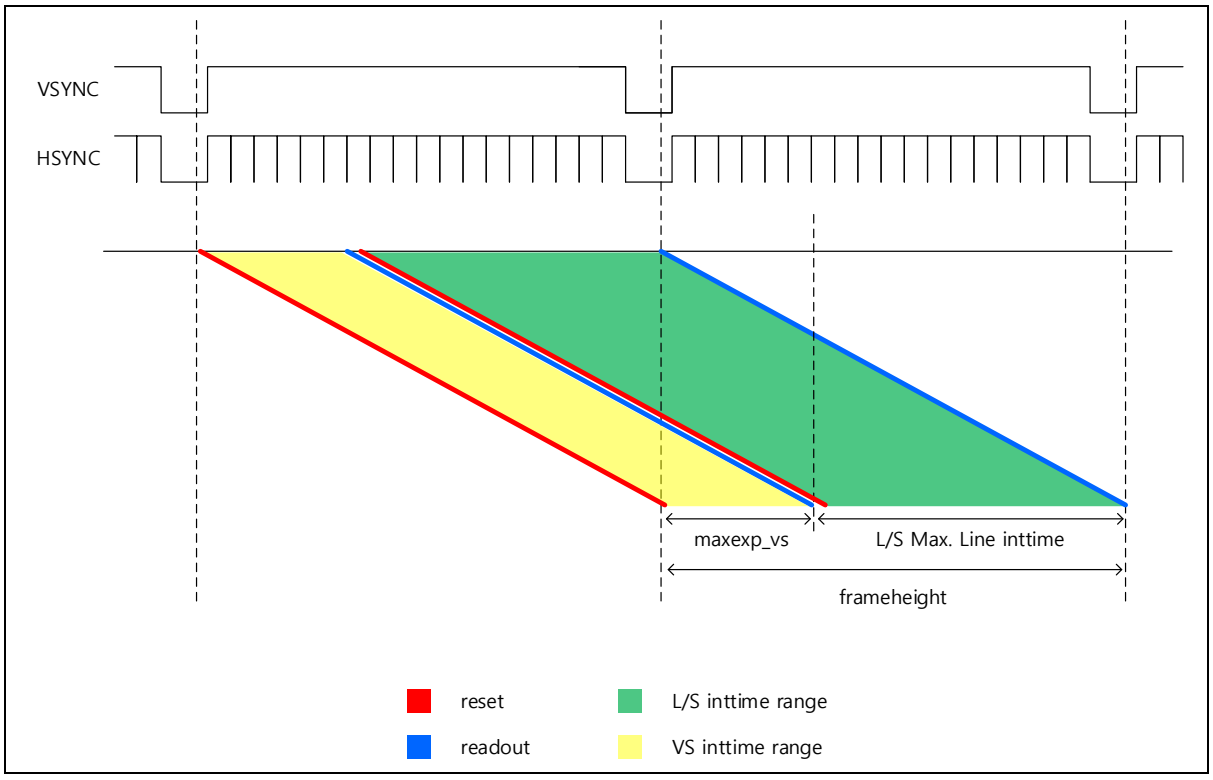
Reset process initializes ROBP region and Effective pixel in row sequence row by row. After reset process, Effective pixel are exposured to light. ROBP region aren't exposured to light. In sequence, readout process reads data of ROBP and Effective pixel. Readout process is identical at order and speed as reset process.

The difference in time between reset and readout process is known as integration time (inttime). The inttime controls time of effective pixel exposured to light. inttime can be adjusted in line unit level (line inttime) and column unit level (column inttime).

The PX6130KA supports four modes of operation and achieves four different brightness images. The operation mode consists of L, S, VS.

Figure 17 shows the intime area operating according to L, S, and VS. Reset and readout operate in order based on VSYNC and HSYNC generated for each frame. It is a staggered exposure time, and L/S and VS have a difference in the inttime. The VS intime range is adjusted to the "maxexp_vs" value. The L/S intime range is an area excluding "maxexp_vs" from frameheight.

Figure 17. Fundamental concept of inttime



Depending on the operating mode, the inttime is adjusted to "inttime" and "inttime_vs". (refer to Table 11)

Table 11. Integration time range

Operation mode	Register name	Line inttime (hex)		Column inttime (hex)	
		max	min	max	Min
L / S	inttime	03D8[a]	0	FF	0
VS	inttime_vs	0008[b]	0	FF	0

a. max line inttime = frameheight – “maxexp_vs” – 5

b. max line inttime = “maxexp_vs” – 2

Table 12 shows registers relevant to integration time.

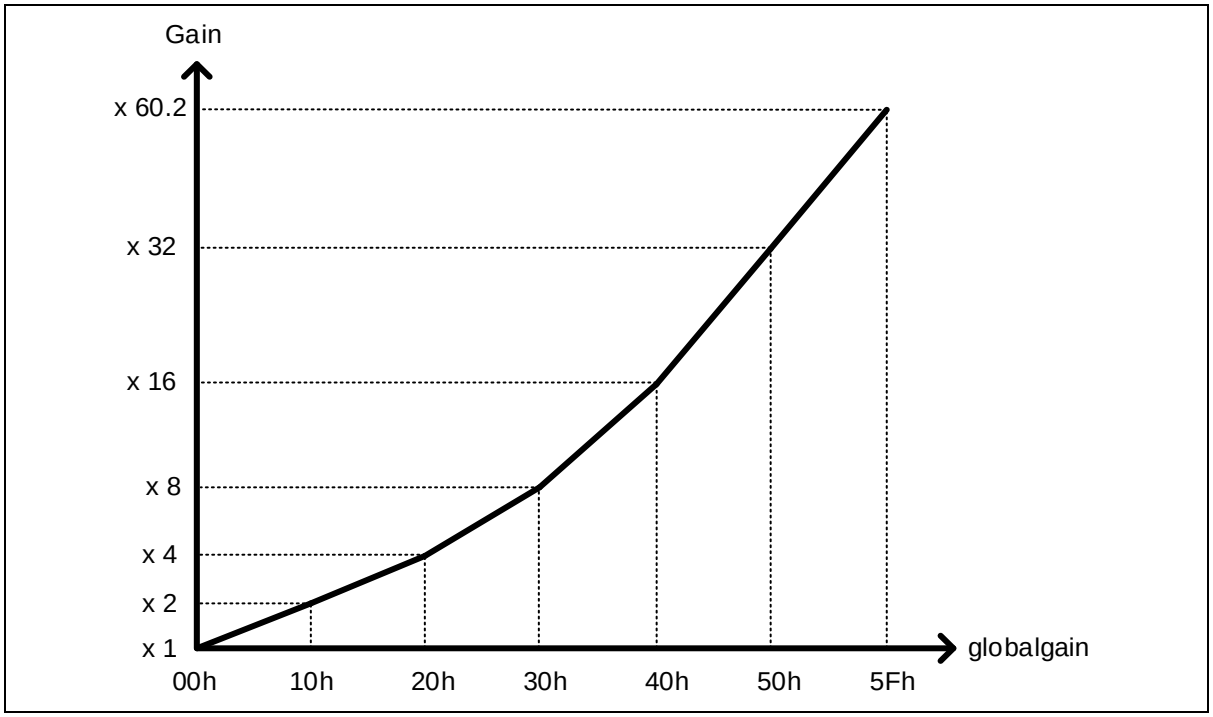
Table 12. Register Table - Integration time

Address	Register Name	R/W	Update	Init Value	Description	
0xF071_0100	maxexp_vs	R/W	AT	8’h0A	[7:0] :	Framewidth High Byte (must be larger than window width)
0xF071_010C	inttime	R/W	AT	24’h014000	[23:16] :	Long Line inttime High Byte
					[15:8] :	Long Line inttime Low Byte
					[7:0] :	Long Column inttime
0xF071_0110	inttime_vs	R/W	AT	24’h000200	[23:16] :	Very short Line inttime High Byte
					[15:8] :	Very short Line inttime Low Byte
					[7:0] :	Very short Column inttime

4.1.1.2. Globalgain

The globalgain is a register for controlling the real gain. It consist of 7bits and control the gain from 1x to 60.2x. MSB 3 bits double gain per code, and LSB 4bits control fine gain from 1x to 1.9x in 16 steps. Figure 18 shows the gain curve of global gain.

Figure 18. Gain curve of Globalgain



Globalgain is divided into three registers in Table 13"globalgain" controls long and short together, "globalgain_vs" controls very short.

Table 13. Register Table - Globalgain

Address	Register Name	R/W	Update	Init Value	Description	
0xF071_1010	globalgain	R/W	AT	8’h0	[7:0] :	Analog gain 0
0xF071_1014	globalgain_vs	R/W	AT	8’h0	[7:0] :	Analog gain 1
0xF071_1018	cds_globalgain	R/W	AT	8’h0	[0] :	Analog gain 0

4.1.1.3. Digital Gain

Analog signal is converted to digital value through ADC operation, and the digital value can be amplified by “digitalgain”. “digitalgain” register's upper 4 bits are positive integer and lower 4 bits are fraction.

Table 14 shows registers relevant to “digitalgain”

Table 14. Register Table - Digital gain

Address	Register Name	R/W	Update	Init Value	Description	
0xF071_1020	digitalgain_l	R/W	AT	8’h10	[7:0] :	Digital gain of long data
0xF071_1024	digitalgain_s	R/W	AT	8’h10	[7:0] :	Digital gain of short data
0xF071_1028	digitalgain_vs	R/W	AT	8’h10	[7:0] :	Digital gain of very short 1 data

4.1.1.4. Exposure factor update control

Depending on "wr_en_off", exposure related registers (integration time, “globalgain”, and “digitalgain”) are updated immediately or when "wr_en" is 1'b1. After setting “wr_en” to 1’b1, you need to change “wr_en” to 1’b0 for the next setting.

Due to exposure related registers split across several registers, if they are changed over several frames, the brightness of the screen changes for each frame, which causes hunting. If exposure related registers are updated at once after writing all register, the brightness of the screen is not changed many times.

Table 15 shows registers relevant to exposure register update

Table 15. Register Table - Exposure register update

Address	Register Name	R/W	Update	Init Value	Description	
0xF071_105C	wr_en	R/W	AT	1’h0	[0] :	Update exposure related register 1'b0 : no update 1'b1 : wr_en set
0xF071_1060	wr_en_off	R/W	AT	1’h0	[0] :	Update exposure related register 1'b0 : update @ wr_en = 1'b1 1'b1 : Immediately update

4.1.2. Test Pattern (TP) Control

TP control generates test images from TG block. Test images type can be selected by setting tp_control_0 registers. In case of test image types from 0x15 to 0x1A values for tp_control_0, tp_control_1/2/3/4 registers are used as color values and the following rule shows how the color value is determined:

R: {tp_control_1_h [1:0], tp_control_1_l}

Gr: {tp_control_2_h [1:0], tp_control_2_l}

Gb: {tp_control_3_h [1:0], tp_control_3_l}

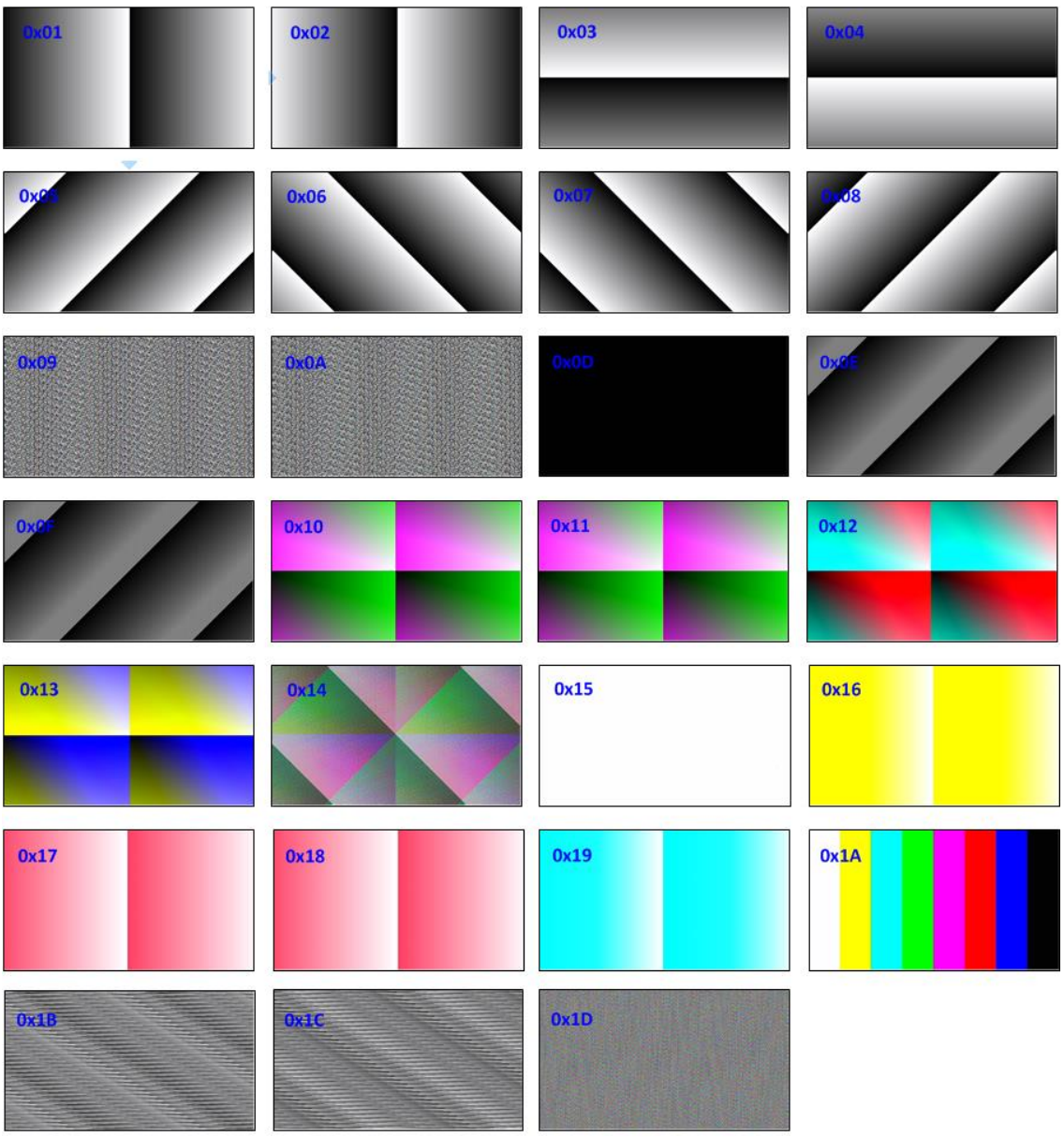
B: {tp_control_4_h [1:0], tp_control_4_l}

Table 16 shows registers relevant to Test Pattern control.

Table 16. Register Table - Test pattern control

Address	Register Name	R/W	Update	Init Value	Description	
0xF071_1070	tp_control_0	R/W	AT	8’h00	[7:0] :	Test pattern selection
0xF071_1074	tp_control_1	R/W	AT	10’h000	[9:8] :	R color for test pattern High Byte
					[7:0] :	R color for test pattern Low Byte
0xF071_1078	tp_control_2	R/W	AT	10’h000	[9:8] :	G1 color for test pattern High Byte
					[7:0] :	G1 color for test pattern Low Byte
0xF071_107C	tp_control_3	R/W	AT	10’h000	[9:8] :	G2 color for test pattern High Byte
					[7:0] :	G2 color for test pattern Low Byte
0xF071_1080	tp_control_4	R/W	AT	10’h000	[9:8] :	B color for test pattern High Byte
					[7:0] :	B color for test pattern Low Byte

Figure 19. Test image



4.1.3. White Balance (WB) gain

The WB gain is functioning that process image in according to color of light source.

R gain[8:0] = {wb_rgain_h[0], wb_rgain_l[7:0]}

G gain[8:0] = {wb_ggain_h[0], wb_ggain_l[7:0]}

B gain[8:0] = {wb_bgain_h[0], wb_bgain_l[7:0]}

The user can change registers to control WB gain. The sequence of bayer pattern is R[0], Gr[1], Gb[2], and B[3]. The WB gain of each channel consists of R, G, and B channel with 9-bit (3i.6f). In the WB gain of R channel, LSB 1-bit of “wb_rgain_h” and MSB 2-bit of “wb_rgain_l” are integer, and LSB 6-bit of “wb_rgain_l” are fraction. If WB gain of R channel is x1, “wb_rgain” is 0x0040. The operation of G and B channel are same such as R channel.

Table 17 shows registers relevant to WB gain control.

Table 17. Register Table – WB gain control

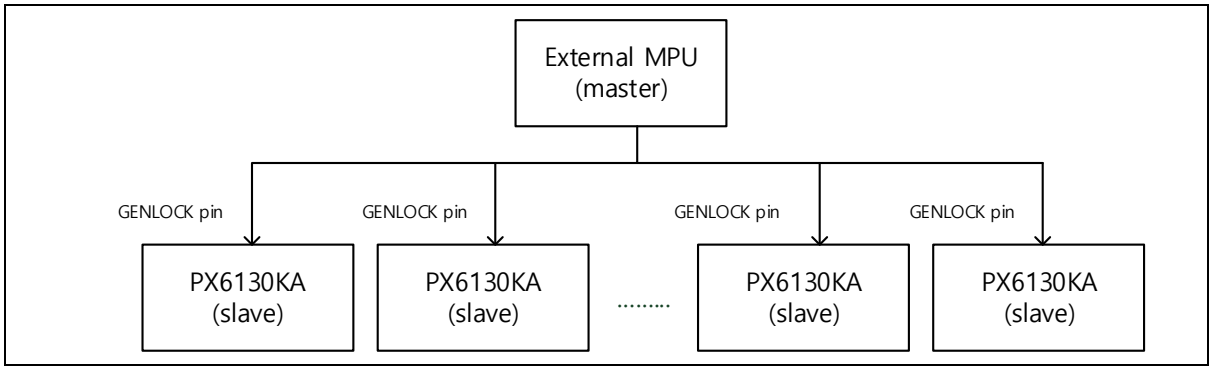
Address	Register Name	R/W	Update	Init Value	Description	
0xF071_0018	[7]wb_en	R/W	AT	1’h0	[7] :	White balance enable control 1'b0 : disable 1'b1 : enable
0xF071_102C	wb_rgain_l	R/W	AT	9’h040	[8] :	White balance "R" gain for long High Byte
					[7:0] :	White balance "R" gain for long Low Byte
0xF071_1030	wb_ggain_l	R/W	AT	9’h040	[8] :	White balance "G" gain for long High Byte
					[7:0] :	White balance "G" gain for long Low Byte
0xF071_1034	wb_bgain_l	R/W	AT	9’h040	[8] :	White balance "B" gain for long High Byte
					[7:0] :	White balance "B" gain for long Low Byte
0xF071_1038	wb_rgain_s	R/W	AT	9’h040	[8] :	White balance "R" gain for short High Byte
					[7:0] :	White balance "R" gain for short Low Byte
0xF071_103C	wb_ggain_s	R/W	AT	9’h040	[8] :	White balance "G" gain for short High Byte
					[7:0] :	White balance "G" gain for short Low Byte
0xF071_1040	wb_bgain_s	R/W	AT	9’h040	[8] :	White balance "B" gain for short High Byte
					[7:0] :	White balance "B" gain for short Low Byte
0xF071_1044	wb_rgain_vs	R/W	AT	9’h040	[8] :	White balance "R" gain for very short 1 High Byte
					[7:0] :	White balance "R" gain for very short 1 Low Byte
0xF071_1048	wb_ggain_vs	R/W	AT	9’h040	[8] :	White balance "G" gain for very short 1 High Byte

Address	Register Name	R/W	Update	Init Value	Description	
					[7:0] :	White balance "G" gain for very short 1 Low Byte
0xF071_104C	wb_bgain_vs	R/W	AT	9’h040	[8] :	White balance "B" gain for very short 1 High Byte
					[7:0] :	White balance "B" gain for very short 1 Low Byte

4.1.4. Genlock

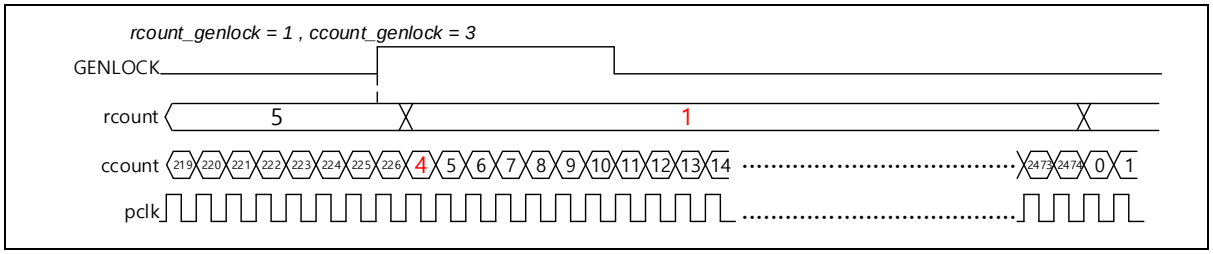
Generator locking (Genlock) function synchronizes internal synchronous timing of master device and slave device.

Figure 20. Genlock Sync configuration with MPU



When PX6130KA receives genlock signal from the master device through GENLOCK PAD, internal row counter and column counter are initialized as “rcount_genlock” and “ccount_genlock” value at the rising edge of genlock signal. Pulse width of genlock signal requires at least 4 pclk period to enable reliable genlock operation.

Figure 21. Genlock timing



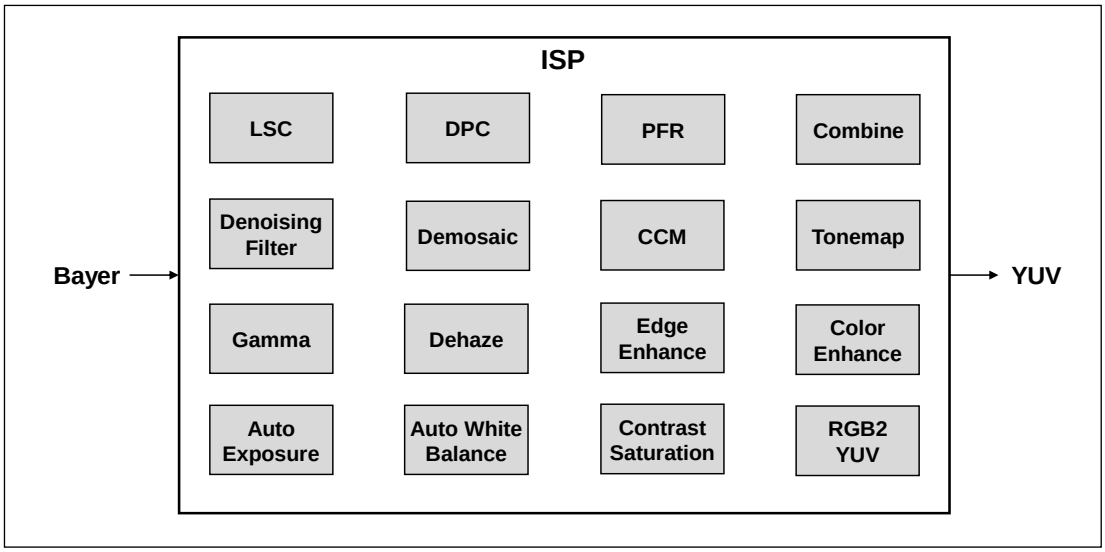
Note If the synchronization timing difference between master and slave is large, sudden shift in brightness may occur in slave device's image.

Table 18. Genlock control

Address	Register Name	R/W	Update	Init Value	Description	
0xF071_0028	genlock_en	R/W	AT	1’h0	[2] :	GENLOCK enable 1'b0 : disable 1'b1 : enable
0xF071_00F0	rcount_genlock	R/W	AT	13’h0001	[12:8] :	Genlock row count High Byte
					[7:0] :	Genlock row count Low Byte
0xF071_00F4	ccount_genlock	R/W	AT	13’h0001	[12:8] :	Genlock column count High Byte
					[7:0] :	Genlock column count Low Byte

4.2. Image Signal Processing (ISP)

Figure 22. ISP function block diagram



The ISP (Image Signal Processor) is an engine that gets raw data from the image sensor, cleans it up and tunes it in a various ways to get a better looking image. The PX6130KA ISP block receives multiple exposure bayer format data from the sensor block and combines those different exposure images of the scene to improve the dynamic range of it. The input bayer data is converted into the RGB data by color interpolation (Demosaic) process. Before RGB conversion, correcting the defective pixel (DPC) and lens shading (LSC), purple fringe (PFR), balancing the color (AWB), optimizing the exposure (AE) and removing the noise functions (Denoising Filter) are performed as a preprocessing. As a HDR sensor, Tonemap process is performed on this stage to get the high dynamic range image. The PX6130KA supports local tonemap algorithm which helps bring out details by increasing contrast in local areas. The RGB data is converted to YUV data after correcting the color (CCM) and gamma. The ISP improves the sharpness (Edge Enhancement), contrast (Adaptive Contrast Enhancement) and color (Color Enhancement) in YUV domain. After globally adjusting contrast, saturation and brightness again, ISP processed image goes out in the YUV format.

The image quality of ISP output is mostly dependent on tuning. Since the preferred images are different for each user, tuning process is important during the system development. To facilitate tuning of parameters, specific ISP tuning tool and tuning guide is provided. The PX6130KA proprietary tuning tool uses I^2C slave port to control the registers in ISP.

Main features of ISP are as below:

- Lens shading correction (LSC)
- Defective pixel correction (DPC)
- Purple fringe reduction (PFR)
- High performance spatial denoising filter(2DNR)
- HDR Combine
- Global and Local Tonemap
- Color interpolation(De-mosaicking)
- Color correction matrix (CCM)
- Gamma correction
- Dehaze

- Adaptive Contrast Enhancement
- Edge Enhancement
- Color Enhancement
- Auto exposure and Auto white balance

4.2.1. LSC (Lens Shading Correction)

The LSC compensates for the dark area of an image corner due to the insufficient amount of light at the edge by the lens. The “lens_scale” value suitable for the lens curvature and different gains are applied to R, Gr, Gb, and B. Figure 23 shows the center adjustment of LSC according to “lens_x” and “lens_y” settings. Figure 24 shows that the lens gain increases according to the distance value from the center.

Figure 23. LSC center control

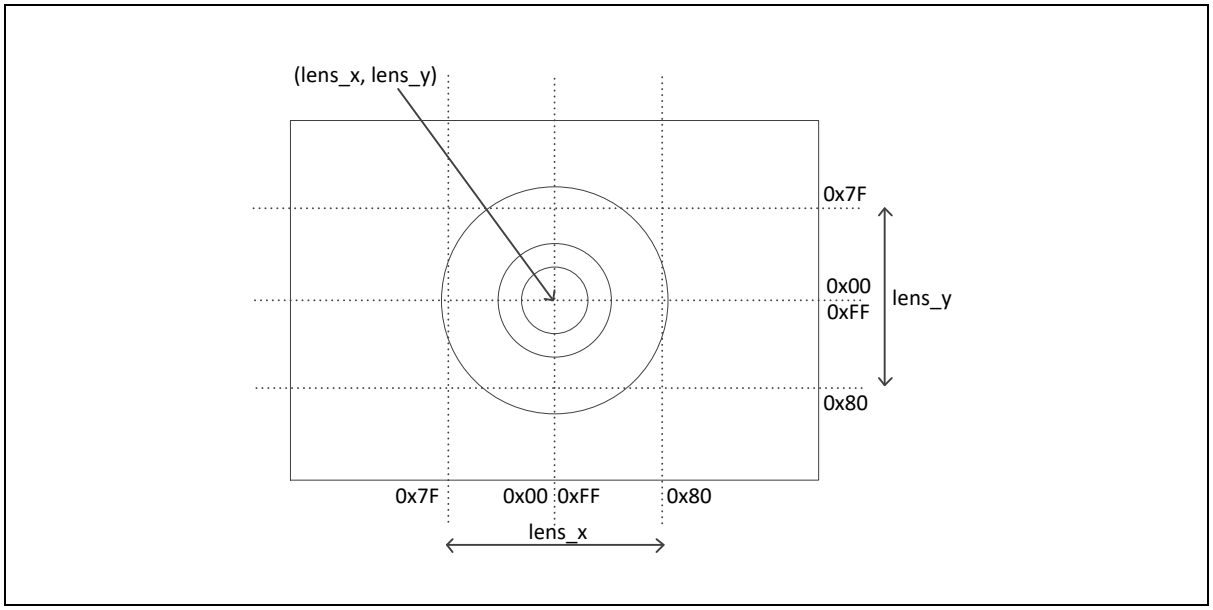
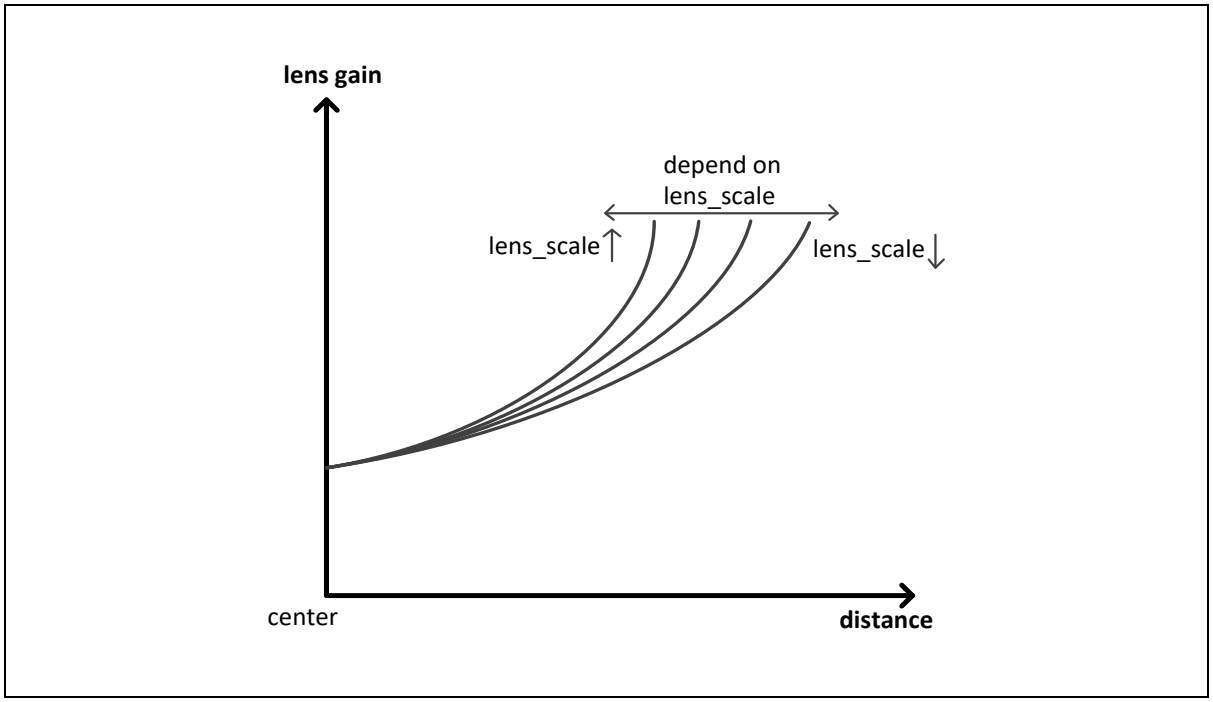


Figure 24. LSC gain fitting with LSC center and LSC scale



4.2.2. DPC

Defective pixels degrade the quality of the images produced by image sensor. If those pixels are not corrected well, demosaicing and denoise filtering operations will cause them to spread and appear as colored clusters that are detrimental to image quality. The PX6130KA adopts a robust DPC (Defective Pixel Correction) algorithm which robustly detects and corrects singlets and couplets of hot pixel, cold pixels or mixture of both types and results in detail-preserving high quality image. The OTP memory also stores the coordinates of 64 defective pixels so that it helps DPC to operate more perfectly.

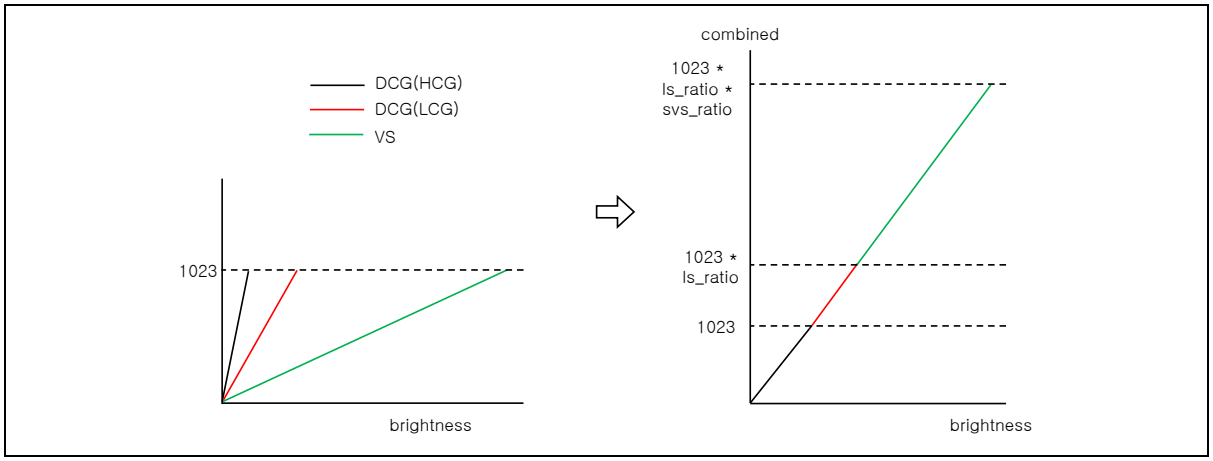
4.2.3. PFR (Purple Fringe Reduction)

Due to the chromatic aberration caused by the difference in R, G, and B wavelength lengths, purple fringing occurs where R and B colors are seen around a white object (especially a light source). The PFR calculates the gradient of purple fringing characteristics, and the PFR intensity can be adjusted through ISP tuning parameter. The PFR can be enabled for Long/Short/Very Short data and for R and B channel respectively.

4.2.4. HDR Combine

The HDR Combine block takes 3 images (Long, Short and Very Short) and combines them into an HDR image. The images are synthesized by applying the respective combine ratios for Long, Short and Very short data. Figure 25 shows the HDR combine concept from 3 images.

Figure 25. HDR combine with 3 images



4.2.5. HDR Tonemap

Since HDR images cannot be expressed in general display devices, HDR images must be converted to SDR (Standard Dynamic Range) images using Tonemap technique. Generally Tonemap is largely classified into Global Tonemap and Local Tonemap technique. The Global Tonemap is a method of redistributing luminance to be suitable for HVS (Human Visual System) according to the whole average luminance level of an image. The Global Tonemap has the advantage of fast processing because it does not require much computation, but it causes a large loss of local data. The Local Tonemap has been proposed to perform tone mapping while preserving local data lost in Global Tonemap. Since the Local Tonemap considers regional values of luminance, it is possible to perform tone mapping while preserving detailed luminance information of an image. However, in an image with a high contrast region, the Local Tonemap may cause halo and banding artifacts around the contours of objects. Each Global and Local Tonemap technique can obtain visually improved SDR images for scenes with limited characteristics, but it is difficult to provide constant high tonemap quality for various scenes. Therefore, to compensate for the disadvantages of the two techniques, mixed tone mapping based approach is adopted to maximally preserve luminance information lost in each Global and Local Tonemap technique.

4.2.6. Denoising Filter

The amount of photons incident on a certain area of the sensor is not constant and random over time, but this random characteristic appears in the form of noise on the image (Shot Noise). This shot noise has a Poisson distribution, and the amount of noise changes according to the level of the signal in proportion to the square root of the average value of the signal. In addition to this shot noise, the noise generated when light is converted into an electrical signal and analog into a digital signal is called Read Out Noise, and this noise has the characteristic of being uniformly distributed regardless of the level of the signal. The Denoising filter removes sensor noise effectively and correct the image with blurring and damaged areas due to sensor noise.

4.2.7. Demosaic (Color Interpolation)

Depending on the shape of the CFA (Color Filter Array), each specific pixel in sensor has different color information such as Red, Blue and Green like a mosaic image. The Demosaic block interpolates and fills the empty part of each pixel with adjacent pixels which performance affects the overall image quality.

4.2.8. CCM (Color Correction Matrix)

The spectral response characteristics between the human eye and CMOS image sensors are different, and the RGB color in sensor is biased due to sensor process characteristics. The Color Correction Matrix is performed to correct this characteristics.

4.2.9. Gamma Correction

The relationship between human eye's sensitivity to light source and the light intensity have an exponential characteristics rather than linear. Since the light sensitivity of a camera has a linear relationship with the input light intensity, the image from the camera must be processed with gamma correction so that the human eye can easily recognize the image. Gamma correction is a non-linear operation performed on the brightness value of the input image, and the brightness value of the output image have an exponential relationship with brightness value of the input image.

4.2.10. Dehaze

Images of outdoor scenes are usually degraded by the turbid medium (e.g., particles, water-droplets) in the atmosphere. Haze, fog, and smoke are such phenomena due to atmospheric absorption and scattering. The irradiance received by the camera from the scene point is attenuated along the line of sight. Furthermore, the incoming light is blended with the airlight (ambient light reflected into the line of sight by atmospheric particles). The degraded images lose the contrast and color fidelity. The Dehaze block makes the blurry images caused by fog or haze clearer.

4.2.11. Adaptive Contrast Enhancement

The purpose of contrast enhancement is to create image with better visual quality by manipulating the pixel intensity of the image. HE (Histogram Equalization) is the most popular amongst all the techniques due to its effectiveness and ease of implementation. HE remaps the gray levels of the image based on the Probability Density Function and hence flattens and stretches the dynamic range of the histogram. Nevertheless, HE suffers from a well-known limitation: mean brightness shifting which results in the generation of unwanted artifacts and gives non-natural looking on the image. Furthermore, saturation effect by HE contributes to loss of information. The Adaptive Contrast Enhancement technique is adopted to overcome the drawbacks of HE. It is able to preserve the mean brightness of the image and reduce the saturation effect and avoid unnatural enhancement and annoying artifacts.

4.2.12. Edge Enhancement

Edge Enhancement excludes the noise from the image and amplifies the just edge information. The adaptive gain control amplifies a small signal large and amplifies a large signal small.

4.2.13. Color Enhancement

When the color is enhanced a lot, the contrast and detail of image may be reduced. Color enhancement has adaptive gain control to prevent a strong color from being oversaturated.

4.2.14. Auto Exposure and Auto White Balance

Auto Exposure adjusts the exposure time of the sensor to automatically adjust the brightness of the subject according to the preset target brightness. Auto White Balance adjusts the color balance by neutralizing the color of reflected light so that a white object always looks white even if the light source changes.

4.3. Video Output Formatter

The PX6130KA supports DVP or MIPI interface for digital video output interface.

Table 19. Register Table - DVP/MIPI Pin Configuration

Address	Register Name	R/W	Update	Init Value	Description
0xF000_1040	IOC_D3	R/W	AT	1’h0	[24] : D3 Pin In/Out Enable 1'b0 : Disable (MIPI or Down) 1'b1 : Enable (DVP)
	IOC_D2	R/W	AT	1’h0	[16] : D2 Pin In/Out Enable 1'b0 : Disable (MIPI or Down) 1'b1 : Enable (DVP)
	IOC_D1	R/W	AT	1’h0	[8] : D1 Pin In/Out Enable 1'b0 : Disable (MIPI or Down) 1'b1 : Enable (DVP)
	IOC_D0	R/W	AT	1’h0	[0] : D0 Pin In/Out Enable 1'b0 : Disable (MIPI or Down) 1'b1 : Enable (DVP)
0xF000_1044	IOC_D7	R/W	AT	1’h0	[24] : D7 Pin In/Out Enable 1'b0 : Disable (Down) 1'b1 : Enable (DVP)
	IOC_D6	R/W	AT	1’h0	[16] : D6 Pin In/Out Enable 1'b0 : Disable (Down) 1'b1 : Enable (DVP)
	IOC_D5	R/W	AT	1’h0	[8] : D5 Pin In/Out Enable 1'b0 : Disable (Down) 1'b1 : Enable (DVP)
	IOC_D4	R/W	AT	1’h0	[0] : D4 Pin In/Out Enable 1'b0 : Disable (Down) 1'b1 : Enable (DVP)
0xF000_1048	IOC_D9	R/W	AT	1’h0	[8] : D9 Pin In/Out Enable 1'b0 : Disable (Down) 1'b1 : Enable (DVP)
	IOC_D8	R/W	AT	1’h0	[0] : D8 Pin In/Out Enable 1'b0 : Disable (Down) 1'b1 : Enable (DVP)
0xF000_1058	IOC_D11	R/W	AT	1’h0	[8] : D11(MPP) Pin In/Out Enable 1'b0 : Disable (Down) 1'b1 : Enable (DVP)
	IOC_D10	R/W	AT	1’h0	[0] : D10(INTR) Pin In/Out Enable 1'b0 : Disable (Down) 1'b1 : Enable (DVP)

4.3.1. DVP Output

The PX6130KA produces RAW data with 10bit / 12bit format and YUV data with 8bit ITU-R BT.656/1120 format. The Table 20 describes the information of DVP pin configuration.

Table 20. DVP Pin Configuration

Pin Name	YCbCr Mode	Bayer Mode	
	8 Bits	10 Bits	12 Bits
D0	YCbCr[0]	Bayer[0]	Bayer[0]
D1	YCbCr[1]	Bayer[1]	Bayer[1]
D2	YCbCr[2]	Bayer[2]	Bayer[2]
D3	YCbCr[3]	Bayer[3]	Bayer[3]
D4	YCbCr[4]	Bayer[4]	Bayer[4]
D5	YCbCr[5]	Bayer[5]	Bayer[5]
D6	YCbCr[6]	Bayer[6]	Bayer[6]
D7	YCbCr[7]	Bayer[7]	Bayer[7]
D8		Bayer[8]	Bayer[8]
D9		Bayer[9]	Bayer[9]
ERR/D10			Bayer[10]
MPP/D11			Bayer[11]

Table 21. Register Table - DVP Format

Address	Register Name	R/W	Update	Init Value	Description	
0xF080_0040	PAR_OUT	R/W	AT	1’h0	[28] :	Output Selection 1'b0 : Bayer Data 1'b1 : YCbCr Data
	PAR_OUT_BW	R/W	AT	2’h0	[11:10]	Bit-width Selection 0 : Reserved 1 : 10 Bits Bayer 2 : 12 Bits Bayer 3 : 8 Bits YCbCr Mode
	EMB_SYNC_EN	R/W	AT	1’h0	[3]	Embedded Sync Enable 0 : Disable 1 : Enable
	EMB_SYNC_MD	R/W	AT	1’h0	[0]	Embedded Sync Mode 0 : BT1120 1 : BT656

The Figure 26 and Figure 27 show the timing diagram of standard ITU-R BT.656/1120 format.

Figure 26. The timing diagram of ITU-R BT.656 format

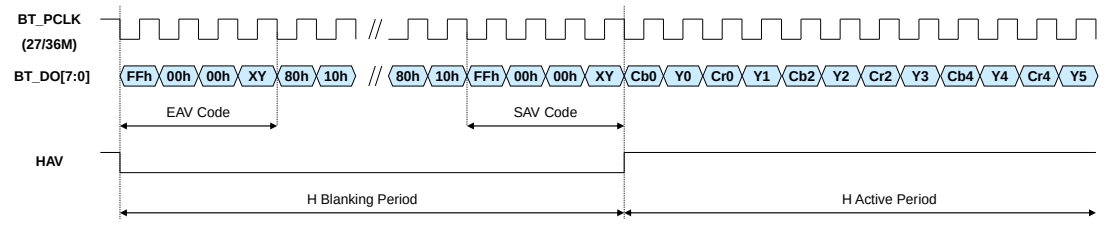
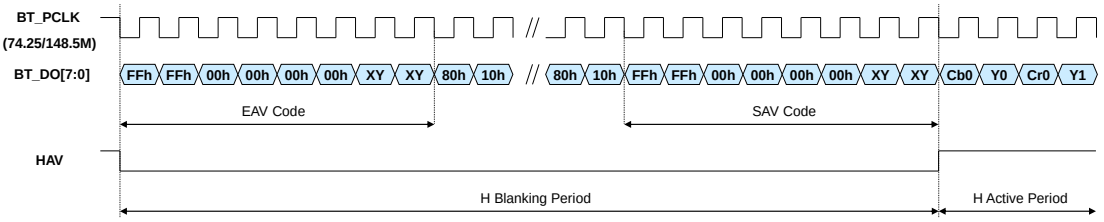


Figure 27. The timing diagram of ITU-R BT.1120 format



4.3.2. MIPI Tx Output

The PX6130KA supports a MIPI interface compliant with MIPI CSI2 V1.00 standard and DPHY V1.00.00 standard with 1 clock lane and 2 data lane. The max data rate of MIPI data lane is up to 600Mbps in HS transmission with RAW 10/12 bits and YUV 422-8bit format.

- Data rate constraints (per lane)
  - Min. : 200 Mbps
  - Max. : 600 Mbps
- Numbers of lanes used : 1-lane, 2-lane (Support Data Lane Swap Function)
- Transmission : Packets are transmitted in HSDT only
- Packets (image format)
  - Short packets : frame start, frame end
  - Long packets : RAW 10-bit, RAW 12-bit, YUV 8-bit
- ECC(Error Correction Code), CRC(Cycle Redundancy Check)

Table 22. Register Table - MIPI Tx Controller Configuration

Address	Register Name	R/W	Update	Init Value	Description	
0xF080_0080	MIPI_PATH_EN	R/W	AT	1’h0	[28] :	MIPI Tx Path Enable 1'b0 : Disable 1'b1 : Enable
	MTX_LANE	R/W	AT	2’h0	[25:24]	MIPI Tx Lane # 0 : 1 Lane 1 : 2 Lane 2/3 : Reserved
	REF_FE_DLY	R/W	AT	14’d0	[13:0]	MIPI Frame End Sync Delay
0xF080_0084	REF_FS_HDLY	R/W	AT	14’d0	[29:16]	MIPI Frame Start Sync Delay
	REF_LS_HDLY	R/W	AT	14’d0	[13:0]	MIPI Line Start Delay
0xF080_0090	MTX_CH_EN	R/W	AT	1’b0	[31]	MTX CH Enable
	CH_BIT_SIZE	R/W	AT	3’b0	[30:28]	Pixel Data Width 1 : 10 Bits Bayer 2 : 12 Bits Bayer 4 : 16 Bits 4:2:2 YCbCr others : Reserved
0xF080_0094	CH_HSIZE	R/W	AT	12’d0	[10:0]	MIPI Output H Size per Line ex) 1280
0xF080_0098	OUT_SIZE_BYTE	R/W	AT	12’d0	[11:0]	MIPI Output Bytes Size per Line ex) 1280x10bit = 1920 B

During MIPI Tx operation, there are two lane states such as Low Power (LP) state and High Speed (HS) state. The HS Tx always drives the lane differentially so that it results in two possible HS lane states such as differential-0 and differential-1. The LP Tx drives two lines of a lane independently with single-ended termination so that it results in four possible LP lane states that are used for Control Mode and Escape Mode. The HS data transmission is used to transfer data in burst mode. It starts from and ends with a stop state (LP-11) of LP Control Mode. The special Escape Mode can only be entered via a request within Control Mode. The data lane shall always exit Escape Mode and return to Control Mode with stop state. If not in HS state or Escape Mode, the data lane shall stay in control mode.

Table 23. Lane State Description of MIPI Transmission

State Code	Line Voltage Levels		High-Speed	Low-Power	
	DP-Line	DN-Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	N/A	N/A
HS-1	HS High	HS Low	Differential-1	N/A	N/A
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	N/A

Figure 28. MIPI Signal Levels for HS and LP State

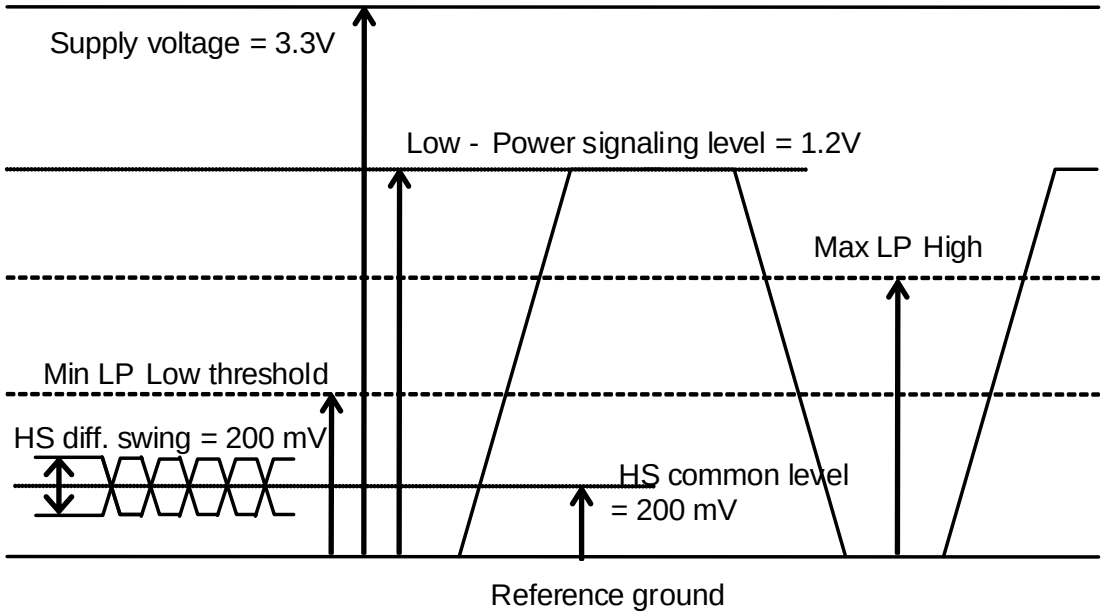


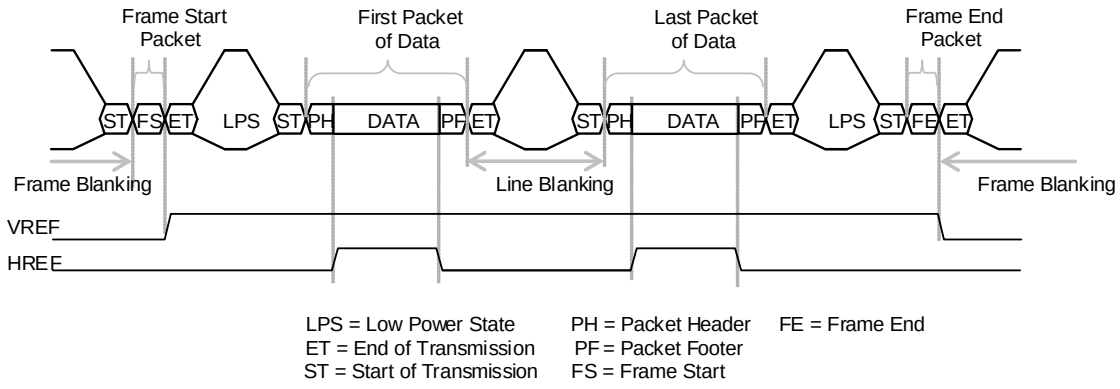
Table 24. Register Table - MIPI Tx PAD Control

Address	Register Name	R/W	Update	Init Value		Description
0xF080_1010	mipi_powerdown	R/W	AT	1’b1	[5]	MIPI DPHY global power down 0 : Disable (Normal) 1 : Power down
	clk_hs_mode	R/W	AT	1’b1	[4]	MIPI Clock lane hs mode 0 : LP & HS mode 1 : Only HS Mode
0xF080_1014	mipi_ck_control	R/W	AT	4’h0	[7:4] :	MIPI CKP/CKN pad state control 4’b0000 : Normal operation 4'b0001 : LP-00 State 4'b0001 : CKP/CKN = LP-00 state + 4'b0010 : CKP/CKN = LP-01 state + 4'b0011 : CKP/CKN = LP-10 state + 4'b0100 : CKP/CKN = LP-11 state + 4'b0101 : CKP/CKN = HS-0 state + 4'b0110 : CKP/CKN = HS-1 state + 4'b0111 : CKP/CKN = Hi-z state + 4'b1000 : CKP/CKN = ULP state + 4'b1010 : CKP/CKN = power down
	mipi_ck_ph	R/W	AT	2’h0	[3:2]	MIPI CKP/CKN Phase control 0/3 : Reserved 1 : Normal 2 : CKP/N Phase Inverted
0xF080_1018	mipi_d0_control	R/W	AT	4’h0	[7:4] :	MIPI DP0/DN0 pad state control 4'b0000 : Normal operation mode 4'b0001 : DP0/DN0 = LP-00 state 4'b0010 : DP0/DN0 = LP-01 state

Address	Register Name	R/W	Update	Init Value	Description
					4'b0011 : DP0/DN0 = LP-10 state 4'b0100 : DP0/DN0 = LP-11 state 4'b0101 : DP0/DN0 = HS-0 state 4'b0110 : DP0/DN0 = HS-1 state 4'b0111 : DP0/DN0 = Hi-z state 4'b1000 : DP0/DN0 = ULP state 4'b1001 : DP0/DN0 = Serializer Test mode 4'b1010 : DP0/DN0 = power down
	mipi_d1_control	R/W	AT	4’h0	[3:0] : MIPI DP1/DN1 pad state control 4'b0000 : Normal operation mode 4'b0001 : DP1/DN1 = LP-00 state 4'b0010 : DP1/DN1 = LP-01 state 4'b0011 : DP1/DN1 = LP-10 state 4'b0100 : DP1/DN1 = LP-11 state 4'b0101 : DP1/DN1 = HS-0 state 4'b0110 : DP1/DN1 = HS-1 state 4'b0111 : DP1/DN1 = Hi-z state 4'b1000 : DP1/DN1 = ULP state 4'b1001 : DP1/DN1 = Serializer Test mode 4'b1010 : DP1/DN1 = power down
0xF080_00D8	mipi_pkt_size_h	R/W	AT	8’h9	[7:0] MIPI Packet Size MSB
0xF080_00DC	mipi_pkt_size_l	R/W	AT	8’h6F	[7:0] MIPI Packet Size LSB
0xF080_1118	mipi_dataid	R/W	AT	8’h0	[7:0] MIPI Data Id [7:6] : Vitual Ch id 0 : Reserved [5:0] : Data Id 6’h1E : YCbCr 4:2:2 8Bits 6’h2B : 10 Bits Bayer 6’h2C : 12 Bits Bayer

The Low Level Protocol (LLP) is a byte oriented, packet based protocol that supports the transport of image data using short and long packet formats. After exiting from the low power state, the Start of Transmission (ST) sequence indicates the start of the packet and the End of Transmission (ET) sequence indicates the end of the packet.

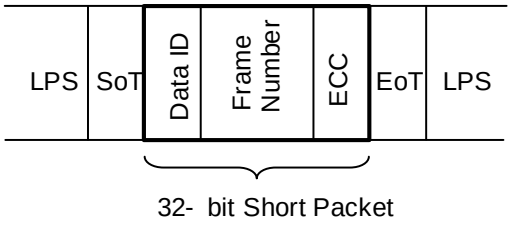
Figure 29. MIPI Low Power Protocol



The PX6130KA supports two kinds of Short packet format for frame synchronization such as Frame Start (FS) packet and Frame End (FE) packet. Each image frame shall begin with a FS packet containing the Frame Start Code. The FS Packet

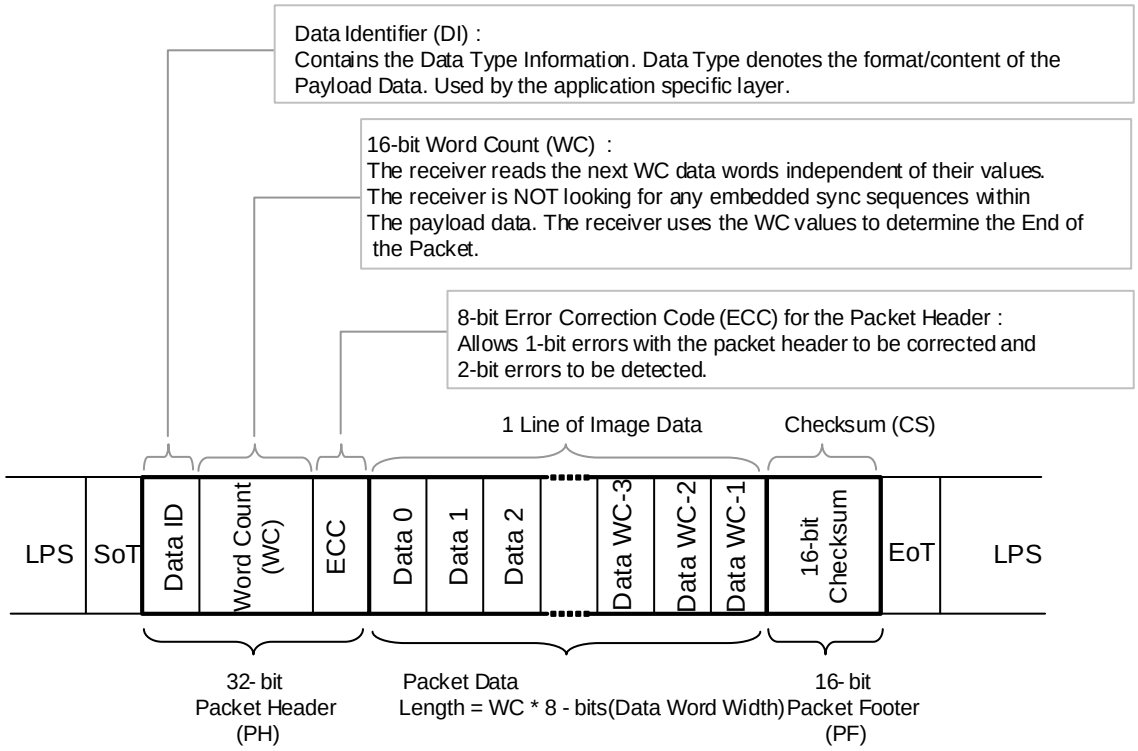
shall be followed by one or more long packets containing image data. Each image frame shall end with the FE packet containing the Frame End Code.

Figure 30. MIPI Short Packet Structure



A Long packet shall consist of 3 elements such as a 32-bit Packet Header (PH), an application Data Payload with a variable number of 8-bit words and a 16-bit Packet Footer (PF).

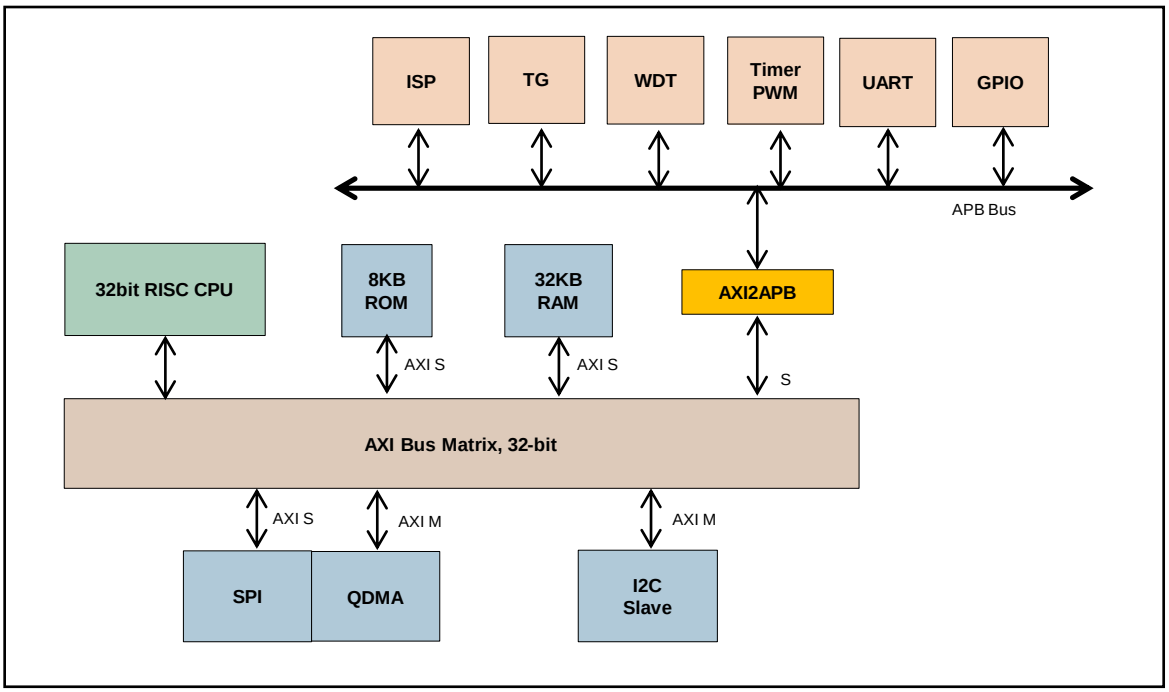
Figure 31. MIPI Long Packet Structure



5. CPU platform

The PX6130KA includes 32bit RISC processors. CPU platform and bus architecture is based on high performance AXI bus protocol. The CPU can access any sub block in the bus according to memory mapped addressing. The detailed CPU platform interconnections are shown in the following figure.

Figure 32. CPU Platform Interconnections



5.1. CPU Platform Main Feature

- 32-bit RISC CPU
- SPI type NOR flash interface
- Watch-Dog Timer
- General SPI master/slave for Flash Memory
- 8 channel timer/PWM
- 1 ports UART
- 1 ports I^2C slave
- 10 ports GPIO

5.2. Boot Sequence

Since the PX6130KA operation is based on CPU, boot sequence is necessary for initialization. During the boot sequence, PX6130KA loads the program code from external SPI flash.

5.3. Flash Interface

Flash memory controller in the PX6130KA accesses the external SPI type flash. For the automotive system, fast booting is necessary and it mostly depends on flash read performance. Since the erase and write flash speed mainly just depends on the internal flash execution time, configurable single mode SPI interface is used for these operations. Other features of PX6130KA flash controller are as below:

- Supports NOR flash memory
- 24 bit address mode
- Max. 256M-byte flash access
- Max. 37.125MHz interface clock

The PX6130KA include general SPI interface that share pin with Flash memory controller. It used for Program, Block Erase and Read Statues of Flash Memory.

5.4. UART Interface

One UART interfaces are built in the PX6130KA and available for debugging and communication with external devices. Main features of the UART are as below:

- Programmable baud rate control: Max. 230400
- HW configurable 16, 32, 64 and 128 bytes Tx/Rx FIFO with DMA
- 5~8 bits per character
- 1, 1.5 and 2 stop bits
- Even, odd and stick parity bits
- Line break, parity error, framing errors and data overrun detection

5.5. I2C Interface

The PX6130KA includes I^2C port which supports slave mode for communication with external Host processor or ISP tuning tool. The pins of I^2C are dedicated and do not have pull-up resistance within the PX6130KA. Therefore, it is necessary to attach pull-up resistance on the outside. Main features of the I^2C are as below:

- Data format
  - 7bit slave device address
    - Slave device address is defined by register setting from SPI Flash and selected by CADDR pin
      - CADDR = 0 : Default slave device address is 8’h34 (address can be defined by register setting)
      - CADDR = 1 : Default slave device address is 8’h36 (address can be defined by register setting)
  - Index Address and Data : 32bit
    - 4 byte index address + 4 byte data
- Speed
  - Fast mode(max. 400Kbit/sec)
  - Standard mode(max. 100Kbit/sec)

5.6. Timers/PWM

There are eight 32-bit timers in the PX6130KA. All eight timers are available for user application, especially fifth ~ eighth timers are connected to PWM (Pulse Width Modulation) function which is used for wide range of purpose. PWM signal can be emitted to outside by alternative pin selection. User can select various timer clocks divided from main clock (27MHz) as range 1/2 to 1/16.

5.7. Watch-Dog Timer

The watch-dog timer is used to reset the whole chip when the firmware runs out of order or some systematic error detected. It is consists 32-bit counter and its clock is selected as the timer clock source.

5.8. General Purpose I/O

The PX6130KA has 10 GPIO (General Purpose I/O) pins. Each pin, which is a bi-directional buffer, may be used in input mode or output mode by program. When each GPIO is used in the input mode, it may be used as an external interrupt source. By signal level or edge fed to GPIO pins, interrupt may be transmitted to PX6130KA CPU. The use of level and edge, and the decision of interrupt source of high/low level and rising/falling edge all may be selected by program.

6. OTP memory

The PX6130KA contains a total of 2K-bit OTP memory. A large portion of 2K-bit are used by PixelPlus for temper sensor, pixel sensitivity deviation correction and x,y coordinates of the OTP DPC. The user can use 128-bit OTP memory. The user can write or read data values with I2C to OTP memory. The user may store necessary information (identification information, etc.) in the OTP memory.

The OTP memory can write or read maximum 128-bit data values at a time. The addresses of the OTP memory that you want to read or write to are set to "otp_addr_start" and "otp_addr_stop"(refer to Table 25). The 128-bit write value is set to "otp_wdata00~otp_wdata15, and the 128-bit read value is stored in "otp_rdata00~otp_rdata15"

Table 25. OTP address

OTP bit	OTP address
[0]	0x00
[1]	0x01
[2]	0x02
-	-
[125]	0x7D
[126]	0x7E
[127]	0x7F

The user must be very careful when writing data values to OTP memory. Because OTP memory can only be used once. If the bit is changed to 1'b1, it can never be returned to 1'b0. So the user should follow the process below.

6.1. The process of reading the OTP memory

The process of reading the OTP memory is as follows.

(1) Set the values of "otp_addr_start" and "otp_addr_stop".

(2) Set the value of "otp_mode_read" to 1'b1.

(3) Check the values from "otp_rdata00" to "otp_rdata15".

6.2. The process of writing to the OTP memory

The process of writing the OTP memory is as follows.

(1) Check that all read values are 1'b0.

(2) Set the values of "otp_addr_start" and "otp_addr_stop".

(3) Set values from "otp_wdata00" to "otp_wdata15".

(4) Set the value of "otp_mode_write" to 1'b1.

(5) Compare the write value and the read value values.

Table 26. OTP

Address	Register Name	R/W	Update	Init Value	Description	
0xF072_0010	otp_mode_read	R/W	AT	1’h0	[5] :	OTP read mode 1'b0 : disable 1'b1 : enable
0xF072_0010	otp_mode_write	R/W	AT	1’h0	[4] :	OTP write mode 1'b0 : disable 1'b1 : enable
0xF072_0020	otp_addr_start	R/W	AT	11’h000	[10:8] :	OTP start address High Byte
					[7:0] :	OTP start address Low Byte
0xF072_0024	otp_addr_stop	R/W	AT	11’h03F	[10:8] :	OTP stop address High Byte
					[7:0] :	OTP stop address Low Byte
0xF072_0028	otp_wdata000	R/W	AT	8’h00	[7:0] :	OTP write data 0
0xF072_002C	otp_wdata001	R/W	AT	8’h00	[7:0] :	OTP write data 1
0xF072_0030	otp_wdata002	R/W	AT	8’h00	[7:0] :	OTP write data 2
0xF072_0034	otp_wdata003	R/W	AT	8’h00	[7:0] :	OTP write data 3
0xF072_0038	otp_wdata004	R/W	AT	8’h00	[7:0] :	OTP write data 4
0xF072_003C	otp_wdata005	R/W	AT	8’h00	[7:0] :	OTP write data 5
0xF072_0040	otp_wdata006	R/W	AT	8’h00	[7:0] :	OTP write data 6
0xF072_0044	otp_wdata007	R/W	AT	8’h00	[7:0] :	OTP write data 7
0xF072_0048	otp_wdata008	R/W	AT	8’h00	[7:0] :	OTP write data 8
0xF072_004C	otp_wdata009	R/W	AT	8’h00	[7:0] :	OTP write data 9
0xF072_0050	otp_wdata010	R/W	AT	8’h00	[7:0] :	OTP write data 10
0xF072_0054	otp_wdata011	R/W	AT	8’h00	[7:0] :	OTP write data 11
0xF072_0058	otp_wdata012	R/W	AT	8’h00	[7:0] :	OTP write data 12
0xF072_005C	otp_wdata013	R/W	AT	8’h00	[7:0] :	OTP write data 13
0xF072_0060	otp_wdata014	R/W	AT	8’h00	[7:0] :	OTP write data 14
0xF072_0064	otp_wdata015	R/W	AT	8’h00	[7:0] :	OTP write data 15
0xF072_1010	otp_rdata000	RO			[7:0] :	OTP read data 0
0xF072_1014	otp_rdata001	RO			[7:0] :	OTP read data 1
0xF072_1018	otp_rdata002	RO			[7:0] :	OTP read data 2
0xF072_101C	otp_rdata003	RO			[7:0] :	OTP read data 3
0xF072_1020	otp_rdata004	RO			[7:0] :	OTP read data 4
0xF072_1024	otp_rdata005	RO			[7:0] :	OTP read data 5
0xF072_1028	otp_rdata006	RO			[7:0] :	OTP read data 6
0xF072_102C	otp_rdata007	RO			[7:0] :	OTP read data 7
0xF072_1030	otp_rdata008	RO			[7:0] :	OTP read data 8
0xF072_1034	otp_rdata009	RO			[7:0] :	OTP read data 9

Address	Register Name	R/W	Update	Init Value	Description
0xF072_1038	otp_rdata010	RO			[7:0] : OTP read data 10
0xF072_103C	otp_rdata011	RO			[7:0] : OTP read data 11
0xF072_1040	otp_rdata012	RO			[7:0] : OTP read data 12
0xF072_1044	otp_rdata013	RO			[7:0] : OTP read data 13
0xF072_1048	otp_rdata014	RO			[7:0] : OTP read data 14
0xF072_104C	otp_rdata015	RO			[7:0] : OTP read data 15

7. Safety concept

The PX6130KA is designed to have safety mechanism to meet ASIL-B capability.

Table 27 shows internal safety mechanism list in the PX6130KA.

Table 27. Safety Mechanism List

ID	Name	Description
SM001	ADC test pattern	Detect faults of Column ADC
SM002	Latch test pattern	Detect timing faults of Column ADC
SM003	Array row control check	Detect faults of Row select
SM004	Array column control check	Detect faults of any column address in an array
SM005	ROBP filter	Compensate defect OBP pixels
SM006	BLC voltage monitoring	Detect faults of Analog BLC voltage
SM007	Digital pattern generator	Generate digital patterns to detect faults in processing of image data
SM008	I2C block CRC check	Detect faults of ISP block by checking CRC
SM009	Embedded data	Embed data of sensor info, error flag and CRC etc.
SM010	Frame counter	Generate 16bit frame counter
SM011	I2C CRC	Detect faults of I2C communication using CRC
SM012	Internal reference voltage monitoring	Detect faults of internal reference voltages
SM013	I2C bus read-back check	Detect faults of I2C writing
SM014	MIPI CRC/ECC	Generate CRC and ECC in MIPI packet
SM015	Defect pixel correction	Compensate defect pixels
SM016	OTP CRC	Detect faults in writing and reading data on OTP
SM017	SRAM CRC	Detect faults in writing and reading data on SRAM
SM018	PLL clock monitor	Detect faults of PLL clock
SM019	SRAM built in self-test	Detect faults of SRAM with built in self-test
SM020	Temperature monitoring	Embed temperature data of Sensor
SM021	Temperature sensor self-test	Detect faults of Temp sensor with built in self-test

SM022	Test pattern rows	Generate digital test pattern rows to detect faults in processing of image data
SM023	I2C register lock	Block I2C registers to avoid unintended access
SM024	VSYNC monitoring in MIPI mode	Generate VSYNC in MIPI mode
SM025	Supply voltage monitor	Monitoring external input power
SM026	SRAM HW ECC	Detect faults of SRAM using HW ECC
SM027	internal window watchdog	Detect faults in processing core using window watchdog
SM028	SPI CRC check	Detect faults in writing and reading on SPI Flash
SM029	CPU operation self test	Detect faults of CPU operation with built in self-test
SM030	I2C pattern test	Detect faults of I2C communication by external I2C master
SM031	Interrupt monitoring	Detect faults of Interrupt service
SM032	APB status monitoring	Detect faults of APB bus
SM033	Program sequence monitoring	Detect faults of Program sequence
SM034	SRAM pattern test	Detect faults in writing and reading in SRAM
SM035	Range check(min-max check)	Detect faults of SW components using Range check
SM036	SPI pattern test	Detect faults of SPI Communication
SM037	Stack overflow/underflow monitoring	Detect faults of overflow/underflow in Stack
SM038	RAM SW CRC	Detect faults of RAM SW controller
SM039	SW Redundancy	Secure redundancy in core SW logics
SM040	Functional timeout monitoring	Detect execution timeouts of SW components
SM041	Timer counter monitoring	Detect faults of PWM timer
SM042	Check value counter	Detect faults of Firmware operation
SM043	External window watchdog	Detect faults of sensor by external widow watchdog

8. Electrical Characteristics

8.1. Absolute Maximum Ratings

AVDD supply voltage:	-0.3 [V] to 4.0 [V]
HVDD supply voltage:	-0.3 [V] to 4.0 [V]
DVDD supply voltage:	-0.3 [V] to 1.8 [V]
DVDDM supply voltage:	-0.3 [V] to 1.8 [V]
DC VTG at any input pin:	-0.3 [V] to HVDD+0.3 [V]
DC VTG at any output pin:	-0.3 [V] to HVDD+0.3 [V]
Storage temperature:	-40°C to +125°C

8.2. DC Characteristics

Table 28. DC characteristics

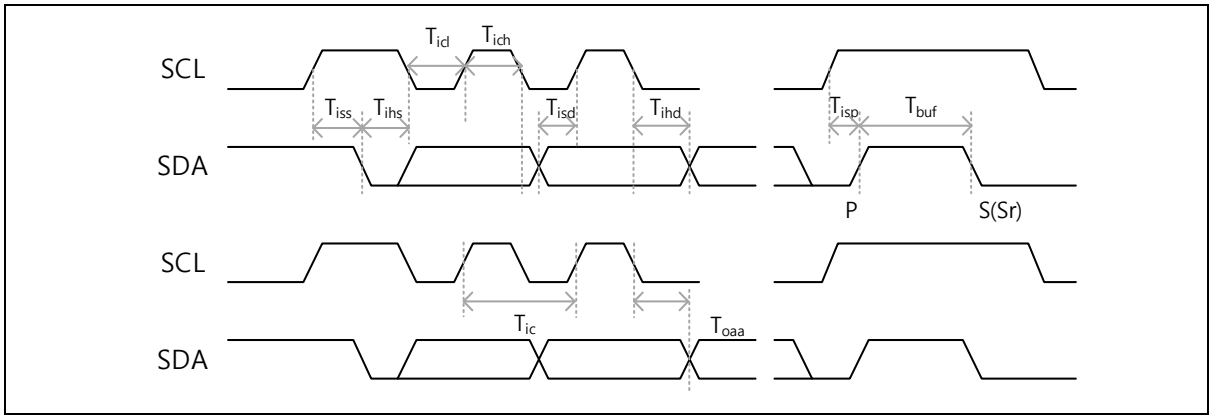
Symbol	Descriptions	Min	Typ	Max	Unit
AVDD	Analog VDD voltage relative to AGND level	TBD	2.8	TBD	[V]
HVDD	IO VDD voltage relative to DGND level	TBD	1.8	TBD	[V]
DVDD	Digital VDD voltage relative to DGND level	TBD	1.2	TBD	[V]
IDDD @ 30fps	HVDD=1.8/2.8 [V] @ DVP	TBD/TBD	TBD/TBD	TBD/TBD	[mA]
	AVDD= 2.8 [V] @ DVP	TBD	TBD	TBD	
	DVDD= 1.2 [V] @ DVP	TBD	TBD	TBD	
	HVDD=1.8/2.8 [V] @ MIPI	TBD/TBD	TBD/TBD	TBD/TBD	
	AVDD = 2.8 [V] @ MIPI	TBD	TBD	TBD	
	DVDD= 1.2 [V] @ MIPI	TBD	TBD	TBD	
IDDS	Standby supply current	TBD	TBD	TBD	[uA]
V_{IL1}	Input voltage low level	-	-	HVDD*0.3	[V]
V_{IH1}	Input voltage high level	HVDD*0.7	-	-	[V]
V_{IL2}	Input voltage low level for rClk, rData.	-	-	HVDD*0.3	[V]
V_{IH2}	Input voltage high level for rClk, rData .	HVDD*0.7	-	-	[V]
C_{IN}	Input pin capacitance	-	-	10	[pF]
V_{OL1}	Output voltage low	-	-	HVDD*0.2	[V]
V_{OH1}	Output voltage high	HVDD*0.8	-	-	[V]
V_{OL2}	Output voltage low level for rClk, rData.	-	-	HVDD*0.2	[V]
V_{OH2}	Output voltage high level for rData.	HVDD*0.8	-	-	[V]
I_{IN}	Input leakage current	-10	-	10	[uA]
I_{OT}	Output leakage current	-10	-	10	[uA]

8.3. AC Characteristics

Table 29. 2-wire serial interface characteristics

Symbol	Descriptions	Min	Typ	Max	Unit
f_{SCLK}	2-wire serial interface Clock frequency	-	-	400	kHz
T_{ic}	2-wire serial interface Clock period	2.5	-	-	us
T_{icl}	2-wire serial interface Clock low level width	1.66	-	-	us
T_{ich}	2-wire serial interface Clock high level width	0.83	-	-	us
T_{iss}	Setup time for start condition	0.83	-	-	us
T_{ihs}	Hold time for start condition	0.83	-	-	us
T_{isd}	Setup time for input data	266	-	-	ns
T_{ihd}	Hold time for input data	-	-	-	ns
T_{isp}	Setup time for stop condition	0.83	-	-	us
T_{buf}	Bus free time between a stop and a new start condition	1.66	-	-	us
T_{oaa}	Delay from SCL falling edge to output data transition	-	-	354	ns
T_r	10% to 90% rising time for SCL/SDA (load : 10pF)	-	-	46	ns
T_f	90% to 10% falling time for SCL/SDA (load : 10pF)	-	-	37	ns
R_p	SCL, SDA pull-up resistor	-	2	-	kΩ

Figure 33. Timing diagram of SCL and SDA



9. Physical specifications (unit : mm)

Figure 34 shows package information, and the package type is A-CSP. Table 30 describes package dimension.

Figure 34. A-CSP Package specifications (top view)

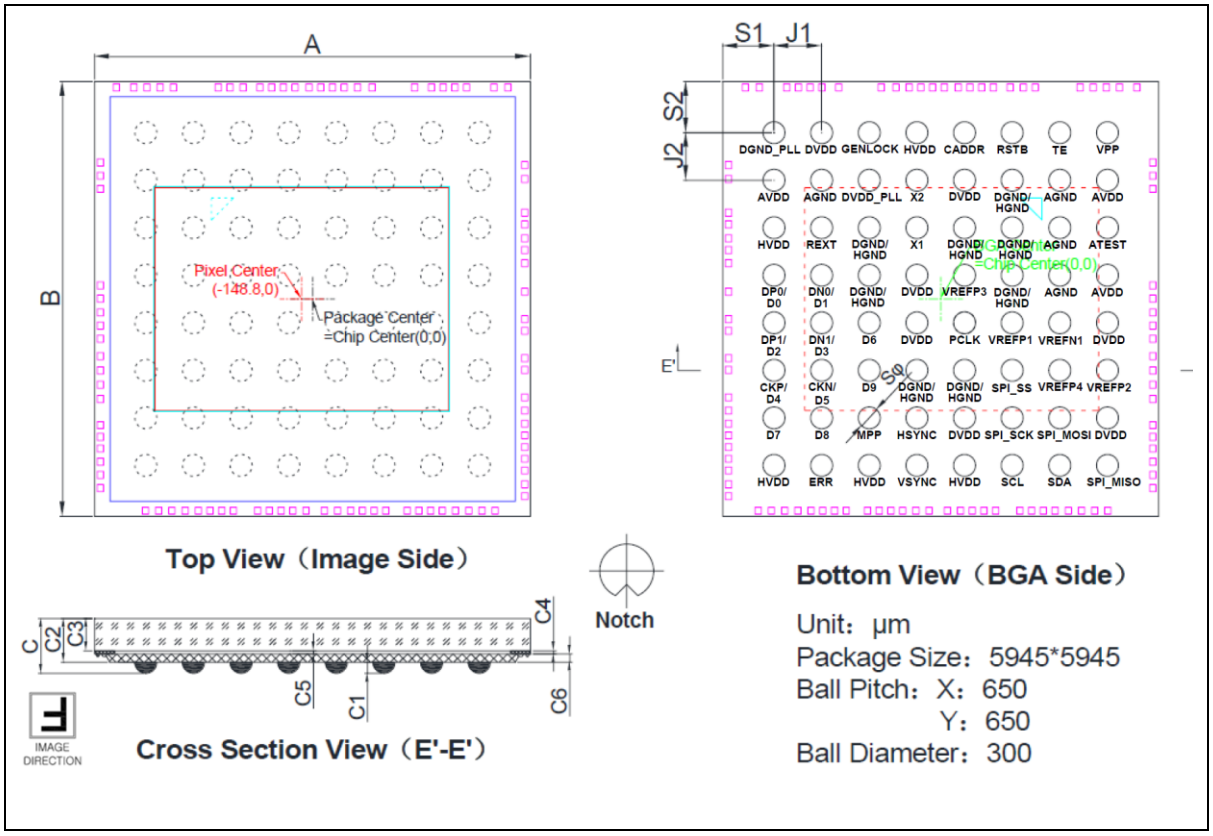


Table 30. Package dimensions

Parameter	Symbol	Nominal	Min	Max	Nominal	Min	Max
			Millimeters			Inches	
Package Body Dimension X	A	5.945	5.92	5.97	0.23406	0.23307	0.23504
Package Body Dimension Y	B	5.945	5.92	5.97	0.23406	0.23307	0.23504
Package Height	C	0.876	0.821	0.931	0.03449	0.03232	0.03665
Cavity wall height	C4	0.041	0.037	0.045	0.00161	0.00146	0.00177
Cavity wall + epoxy thickness (glass to the wafer bonding top point)	C5	0.0435	0.0385	0.0485	0.00171	0.00152	0.00191
Si thickness	C6	0.15	0.14	0.16	0.00591	0.00551	0.0063
Glass Thickness	C3	0.4	0.39	0.41	0.01575	0.01535	0.01614
Package Body Thickness	C2	0.626	0.591	0.661	0.02465	0.02327	0.02602
Ball Height	C1	0.25	0.22	0.28	0.00984	0.00866	0.01102
Ball Diameter		0.3	0.27	0.33	0.01181	0.01063	0.01299
Total Ball Count	N	64					

Ball Count X axis	N1	8					
Ball Count Y axis	N2	8					
Pin Pitch X axis	J1	0.65	0.64	0.66	0.02559	0.0252	0.02598
Pin Pitch Y axis	J2	0.65	0.64	0.66	0.02559	0.0252	0.02598
BGA ball center to package center offset in X-direction	X	0	-0.0250	0.025	0	-0.00098	0.00098
BGA ball center to package center offset in Y-direction	Y	0	-0.0250	0.025	0	-0.00098	0.00098
Edge to Ball Center Distance along X	S1	0.6975	0.6675	0.7275	0.02746	0.02628	0.02864
Edge to Ball Center Distance along Y	S2	0.6975	0.6675	0.7275	0.02746	0.02628	0.02864

10. Register Map

Table 31. Register Table - Frame structure

Address	Register Name	R/W	Update	Init Value	Description	
0xF070_0010	framewidth	R/W	AT	13’h9AA	[12:8] :	Framewidth High Byte (must be larger than window width)
					[7:0] :	Framewidth Low Byte (must be larger than window width)
0xF070_0014	fheight	R/W	AT	13’h3E7	[12:8] :	Frameheight High Byte (must be larger than window height)
					[7:0] :	Frameheight Low Byte (must be larger than window height)
0xF060_4010	prewin_x1	RW	AT	11’h14	[26:16]	Internal horizontal cropping start point
	prewin_x2			11’h524	[10:0]	Internal horizontal cropping end point
0xF071_006C	rjump_top	R/W	AT	13’h014	[12:8]	Row jump top value High Byte
					[7:0] :	Row jump top value Low Byte
0xF071_0070	rjump_bot	R/W	AT	13’h014	[12:8]	Row jump bottom value High Byte
					[7:0] :	Row jump bottom value Low Byte
0xF064_1010	wndow_x1	RW	AT	11’h008	[26:16]	Output horizontal cropping start point
	wndow_x2			11’h508	[10:0]	Output horizontal cropping end point
0xF064_1014	window_y1	RW	AT	11’h008	[26:16]	Output vertical cropping start point
	window_y2			11’h3C8	[10:0]	Output vertical cropping end point

Table 32. Register Table - Mirror

Address	Register Name	R/W	Update	Init Value	Description	
0xF070_016C	mirror	R/W	AT	2’h0	[1:0] :	Image Inversion mirror [1]: vertical inversion mirror [0]: horizontal inversion

Table 33. Register Table - Integration Time

Address	Register Name	R/W	Update	Init Value	Description	
0xF071_0100	maxexp_vs	R/W	AT	8’h0A	[7:0] :	Framewidth High Byte (must be larger than window width)
0xF071_010C	inttime	R/W	AT	24’h014000	[23:16] :	Long Line inttime High Byte
					[15:8] :	Long Line inttime Low Byte

Address	Register Name	R/W	Update	Init Value	Description	
					[7:0] :	Long Column inttime
0xF071_0110	inttime_vs	R/W	AT	24’h000200	[23:16] :	Very short Line inttime High Byte
					[15:8] :	Very short Line inttime Low Byte
					[7:0] :	Very short Column inttime

Table 34. Register Table - Digital Gain

Address	Register Name	R/W	Update	Init Value	Description	
0xF071_1020	digitalgain_l	R/W	AT	8’h10	[7:0] :	Digital gain of long data
0xF071_1024	digitalgain_s	R/W	AT	8’h10	[7:0] :	Digital gain of short data
0xF071_1028	digitalgain_vs	R/W	AT	8’h10	[7:0] :	Digital gain of very short 1 data

Table 35. Register Table - Exposure Register Update

Address	Register Name	R/W	Update	Init Value	Description	
0xF071_105C	wr_en	R/W	AT	1’h0	[0] :	Update exposure related register 1'b0 : no update 1'b1 : wr_en set
0xF071_1060	wr_en_off	R/W	AT	1’h0	[0] :	Update exposure related register 1'b0 : update @ wr_en = 1'b1 1'b1 : Immediately update

Table 36. Register Table - Test Pattern Control

Address	Register Name	R/W	Update	Init Value	Description	
0xF071_1070	tp_control_0	R/W	AT	8’h00	[7:0] :	Test pattern selection
0xF071_1074	tp_control_1	R/W	AT	10’h000	[9:8] :	R color for test pattern High Byte
					[7:0] :	R color for test pattern Low Byte
0xF071_1078	tp_control_2	R/W	AT	10’h000	[9:8] :	G1 color for test pattern High Byte
					[7:0] :	G1 color for test pattern Low Byte
0xF071_107C	tp_control_3	R/W	AT	10’h000	[9:8] :	G2 color for test pattern High Byte
					[7:0] :	G2 color for test pattern Low Byte
0xF071_1080	tp_control_4	R/W	AT	10’h000	[9:8] :	B color for test pattern High Byte
					[7:0] :	B color for test pattern Low Byte

Table 37. Register Table - WB Gain Control

Address	Register Name	R/W	Update	Init Value	Description	
0xF071_0018	[7]wb_en	R/W	AT	1’h0	[7] :	White balance enable control 1'b0 : disable 1'b1 : enable
0xF071_102C	wb_rgain_l	R/W	AT	9’h040	[8] :	White balance "R" gain for long High Byte
					[7:0] :	White balance "R" gain for long Low Byte
0xF071_1030	wb_ggain_l	R/W	AT	9’h040	[8] :	White balance "G" gain for long High Byte
					[7:0] :	White balance "G" gain for long Low Byte
0xF071_1034	wb_bgain_l	R/W	AT	9’h040	[8] :	White balance "B" gain for long High Byte
					[7:0] :	White balance "B" gain for long Low Byte
0xF071_1038	wb_rgain_s	R/W	AT	9’h040	[8] :	White balance "R" gain for short High Byte
					[7:0] :	White balance "R" gain for short Low Byte
0xF071_103C	wb_ggain_s	R/W	AT	9’h040	[8] :	White balance "G" gain for short High Byte
					[7:0] :	White balance "G" gain for short Low Byte
0xF071_1040	wb_bgain_s	R/W	AT	9’h040	[8] :	White balance "B" gain for short High Byte
					[7:0] :	White balance "B" gain for short Low Byte
0xF071_1044	wb_rgain_vs	R/W	AT	9’h040	[8] :	White balance "R" gain for very short 1 High Byte
					[7:0] :	White balance "R" gain for very short 1 Low Byte
0xF071_1048	wb_ggain_vs	R/W	AT	9’h040	[8] :	White balance "G" gain for very short 1 High Byte
					[7:0] :	White balance "G" gain for very short 1 Low Byte
0xF071_104C	wb_bgain_vs	R/W	AT	9’h040	[8] :	White balance "B" gain for very short 1 High Byte
					[7:0] :	White balance "B" gain for very short 1 Low Byte

Table 38. Register Table - Genlock Control

Address	Register Name	R/W	Update	Init Value	Description	
0xF071_0028	genlock_en	R/W	AT	1’h0	[2] :	GENLOCK enable

Address	Register Name	R/W	Update	Init Value	Description	
						1'b0 : disable 1'b1 : enable
0xF071_00F0	rcount_genlock	R/W	AT	13’h0001	[12:8] :	Genlock row count High Byte
					[7:0] :	Genlock row count Low Byte
0xF071_00F4	ccount_genlock	R/W	AT	13’h0001	[12:8] :	Genlock column count High Byte
					[7:0] :	Genlock column count Low Byte

Table 39. Register Table - DVP/MIPI Pin Configuration

Address	Register Name	R/W	Update	Init Value	Description	
0xF000_1040	IOC_D3	R/W	AT	1’h0	[24] :	D3 Pin In/Out Enable 1'b0 : Disable (MIPI or Down) 1'b1 : Enable (DVP)
	IOC_D2	R/W	AT	1’h0	[16] :	D2 Pin In/Out Enable 1'b0 : Disable (MIPI or Down) 1'b1 : Enable (DVP)
	IOC_D1	R/W	AT	1’h0	[8] :	D1 Pin In/Out Enable 1'b0 : Disable (MIPI or Down) 1'b1 : Enable (DVP)
	IOC_D0	R/W	AT	1’h0	[0] :	D0 Pin In/Out Enable 1'b0 : Disable (MIPI or Down) 1'b1 : Enable (DVP)
0xF000_1044	IOC_D7	R/W	AT	1’h0	[24] :	D7 Pin In/Out Enable 1'b0 : Disable (Down) 1'b1 : Enable (DVP)
	IOC_D6	R/W	AT	1’h0	[16] :	D6 Pin In/Out Enable 1'b0 : Disable (Down) 1'b1 : Enable (DVP)
	IOC_D5	R/W	AT	1’h0	[8] :	D5 Pin In/Out Enable 1'b0 : Disable (Down) 1'b1 : Enable (DVP)
	IOC_D4	R/W	AT	1’h0	[0] :	D4 Pin In/Out Enable 1'b0 : Disable (Down) 1'b1 : Enable (DVP)
0xF000_1048	IOC_D9	R/W	AT	1’h0	[8] :	D9 Pin In/Out Enable 1'b0 : Disable (Down) 1'b1 : Enable (DVP)
	IOC_D8	R/W	AT	1’h0	[0] :	D8 Pin In/Out Enable 1'b0 : Disable (Down) 1'b1 : Enable (DVP)
0xF000_1058	IOC_D11	R/W	AT	1’h0	[8] :	D11(MPP) Pin In/Out Enable 1'b0 : Disable (Down) 1'b1 : Enable (DVP)
	IOC_D10	R/W	AT	1’h0	[0] :	D10(INTR) Pin In/Out Enable 1'b0 : Disable (Down) 1'b1 : Enable (DVP)

Table 40. Register Table - DVP Format

Address	Register Name	R/W	Update	Init Value	Description	
0xF080_0040	PAR_OUT	R/W	AT	1’h0	[28] :	Output Selection 1'b0 : Bayer Data 1'b1 : YCbCr Data
	PAR_OUT_BW	R/W	AT	2’h0	[11:10]	Bit-width Selection 0 : Reserved 1 : 10 Bits Bayer 2 : 12 Bits Bayer 3 : 8 Bits YCbCr Mode
	EMB_SYNC_EN	R/W	AT	1’h0	[3]	Embedded Sync Enable 0 : Disable 1 : Enable
	EMB_SYNC_MD	R/W	AT	1’h0	[0]	Embedded Sync Mode 0 : BT1120 1 : BT656

Table 41. Register Table - MIPI Tx Controller Configuration

Address	Register Name	R/W	Update	Init Value	Description	
0xF080_0080	MIPI_PATH_EN	R/W	AT	1’h0	[28] :	MIPI Tx Path Enable 1'b0 : Disable 1'b1 : Enable
	MTX_LANE	R/W	AT	2’h0	[25:24]	MIPI Tx Lane # 0 : 1 Lane 1 : 2 Lane 2/3 : Reserved
	REF_FE_DLY	R/W	AT	14’d0	[13:0]	MIPI Frame End Sync Delay
0xF080_0084	REF_FS_HDLY	R/W	AT	14’d0	[29:16]	MIPI Frame Start Sync Delay
	REF_LS_HDLY	R/W	AT	14’d0	[13:0]	MIPI Line Start Delay
0xF080_0090	MTX_CH_EN	R/W	AT	1’b0	[31]	MTX CH Enable
	CH_BIT_SIZE	R/W	AT	3’b0	[30:28]	Pixel Data Width 1 : 10 Bits Bayer 2 : 12 Bits Bayer 4 : 16 Bits 4:2:2 YCbCr others : Reserved
0xF080_0094	CH_HSIZE	R/W	AT	12’d0	[10:0]	MIPI Output H Size per Line ex) 1280
0xF080_0098	OUT_SIZE_BYTE	R/W	AT	12’d0	[11:0]	MIPI Output Bytes Size per Line ex) 1280x10bit = 1920 B

Table 42. Register Table - MIPI Tx PAD Control

Address	Register Name	R/W	Update	Init Value	Description	
0xF080_1010	mipi_powerdown	R/W	AT	1’b1	[5]	MIPI DPHY global power down 0 : Disable (Normal) 1 : Power down

Address	Register Name	R/W	Update	Init Value		Description
	clk_hs_mode	R/W	AT	1’b1	[4]	MIPI Clock lane hs mode 0 : LP & HS mode 1 : Only HS Mode
0xF080_1014	mipi_ck_control	R/W	AT	4’h0	[7:4] :	MIPI CKP/CKN pad state control 4’b0000 : Normal operation 4'b0001 : LP-00 State 4'b0001 : CKP/CKN = LP-00 state + 4'b0010 : CKP/CKN = LP-01 state + 4'b0011 : CKP/CKN = LP-10 state + 4'b0100 : CKP/CKN = LP-11 state + 4'b0101 : CKP/CKN = HS-0 state + 4'b0110 : CKP/CKN = HS-1 state + 4'b0111 : CKP/CKN = Hi-z state + 4'b1000 : CKP/CKN = ULP state + 4'b1010 : CKP/CKN = power down
	mipi_ck_ph	R/W	AT	2’h0	[3:2]	MIPI CKP/CKN Phase control 0/3 : Reserved 1 : Normal 2 : CKP/N Phase Inverted
0xF080_1018	mipi_d0_control	R/W	AT	4’h0	[7:4] :	MIPI DP0/DN0 pad state control 4'b0000 : Normal operation mode 4'b0001 : DP0/DN0 = LP-00 state 4'b0010 : DP0/DN0 = LP-01 state 4'b0011 : DP0/DN0 = LP-10 state 4'b0100 : DP0/DN0 = LP-11 state 4'b0101 : DP0/DN0 = HS-0 state 4'b0110 : DP0/DN0 = HS-1 state 4'b0111 : DP0/DN0 = Hi-z state 4'b1000 : DP0/DN0 = ULP state 4'b1001 : DP0/DN0 = Serializer Test mode 4'b1010 : DP0/DN0 = power down
	mipi_d1_control	R/W	AT	4’h0	[3:0] :	MIPI DP1/DN1 pad state control 4'b0000 : Normal operation mode 4'b0001 : DP1/DN1 = LP-00 state 4'b0010 : DP1/DN1 = LP-01 state 4'b0011 : DP1/DN1 = LP-10 state 4'b0100 : DP1/DN1 = LP-11 state 4'b0101 : DP1/DN1 = HS-0 state 4'b0110 : DP1/DN1 = HS-1 state 4'b0111 : DP1/DN1 = Hi-z state 4'b1000 : DP1/DN1 = ULP state 4'b1001 : DP1/DN1 = Serializer Test mode 4'b1010 : DP1/DN1 = power down
0xF080_00D8	mipi_pkt_size_h	R/W	AT	8’h9	[7:0]	MIPI Packet Size MSB
0xF080_00DC	mipi_pkt_size_l	R/W	AT	8’h6F	[7:0]	MIPI Packet Size LSB
0xF080_1118	mipi_dataid	R/W	AT	8’h0	[7:0]	MIPI Data Id [7:6] : Vitual Ch id 0 : Reserved [5:0] : Data Id 6’h1E : YCbCr 4:2:2 8Bits 6’h2B : 10 Bits Bayer 6’h2C : 12 Bits Bayer

Table 43. Register Table - OTP

Address	Register Name	R/W	Update	Init Value	Description	
0xF072_0010	otp_mode_read	R/W	AT	1’h0	[5] :	OTP read mode 1'b0 : disable 1'b1 : enable
0xF072_0010	otp_mode_write	R/W	AT	1’h0	[4] :	OTP write mode 1'b0 : disable 1'b1 : enable
0xF072_0020	otp_addr_start	R/W	AT	11’h000	[10:8] :	OTP start address High Byte
					[7:0] :	OTP start address Low Byte
0xF072_0024	otp_addr_stop	R/W	AT	11’h03F	[10:8] :	OTP stop address High Byte
					[7:0] :	OTP stop address Low Byte
0xF072_0028	otp_wdata000	R/W	AT	8’h00	[7:0] :	OTP write data 0
0xF072_002C	otp_wdata001	R/W	AT	8’h00	[7:0] :	OTP write data 1
0xF072_0030	otp_wdata002	R/W	AT	8’h00	[7:0] :	OTP write data 2
0xF072_0034	otp_wdata003	R/W	AT	8’h00	[7:0] :	OTP write data 3
0xF072_0038	otp_wdata004	R/W	AT	8’h00	[7:0] :	OTP write data 4
0xF072_003C	otp_wdata005	R/W	AT	8’h00	[7:0] :	OTP write data 5
0xF072_0040	otp_wdata006	R/W	AT	8’h00	[7:0] :	OTP write data 6
0xF072_0044	otp_wdata007	R/W	AT	8’h00	[7:0] :	OTP write data 7
0xF072_0048	otp_wdata008	R/W	AT	8’h00	[7:0] :	OTP write data 8
0xF072_004C	otp_wdata009	R/W	AT	8’h00	[7:0] :	OTP write data 9
0xF072_0050	otp_wdata010	R/W	AT	8’h00	[7:0] :	OTP write data 10
0xF072_0054	otp_wdata011	R/W	AT	8’h00	[7:0] :	OTP write data 11
0xF072_0058	otp_wdata012	R/W	AT	8’h00	[7:0] :	OTP write data 12
0xF072_005C	otp_wdata013	R/W	AT	8’h00	[7:0] :	OTP write data 13
0xF072_0060	otp_wdata014	R/W	AT	8’h00	[7:0] :	OTP write data 14
0xF072_0064	otp_wdata015	R/W	AT	8’h00	[7:0] :	OTP write data 15
0xF072_1010	otp_rdata000	RO			[7:0] :	OTP read data 0
0xF072_1014	otp_rdata001	RO			[7:0] :	OTP read data 1
0xF072_1018	otp_rdata002	RO			[7:0] :	OTP read data 2
0xF072_101C	otp_rdata003	RO			[7:0] :	OTP read data 3
0xF072_1020	otp_rdata004	RO			[7:0] :	OTP read data 4
0xF072_1024	otp_rdata005	RO			[7:0] :	OTP read data 5
0xF072_1028	otp_rdata006	RO			[7:0] :	OTP read data 6
0xF072_102C	otp_rdata007	RO			[7:0] :	OTP read data 7
0xF072_1030	otp_rdata008	RO			[7:0] :	OTP read data 8
0xF072_1034	otp_rdata009	RO			[7:0] :	OTP read data 9

Address	Register Name	R/W	Update	Init Value	Description
0xF072_1038	otp_rdata010	RO			[7:0] : OTP read data 10
0xF072_103C	otp_rdata011	RO			[7:0] : OTP read data 11
0xF072_1040	otp_rdata012	RO			[7:0] : OTP read data 12
0xF072_1044	otp_rdata013	RO			[7:0] : OTP read data 13
0xF072_1048	otp_rdata014	RO			[7:0] : OTP read data 14
0xF072_104C	otp_rdata015	RO			[7:0] : OTP read data 15

Revision history

Version	Date	Description
V0.1	2023.05.24	Initial Release