DCOD

DL257

EX-SDI Rx / MIPI Tx

Version 1.0

Apr, 2022

Revision History

Version	Date	Description	Modified by
1.0	2022.04.08	Initial release.	H.J. Lee

Document Description

This is the document to describe a feature and register which is applied to DL257.

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Contents

1. General Descriptions & Features

1.1 General Descriptions

The DL257 device is a dedicated automotive chip and is a dual-channel SDI receiver that targets to provide optimum performance with EX-SDI technology in automotive environments.

It has both MIPI-CSI2 and DVP (Parallel) as an output interface with SoC. The EX-SDI is a visually lossless codec for Long Reach Solution, reducing transmission bandwidth to deliver data on inexpensive cables. The DL257 enables high quality digital transmission through PoC(Power over Coax), UCC(Upstream Com. Channel) and ancillary data interfaces to provide optimal performance and functionality in the automotive environment.

1.2 Features

Functions

- Supports EX-SDI decoding
  - ✓ EX-SDI V2.0 - 135Mbps bandwidth
  - ✓ EX-SDI V1.0 - 270Mbps bandwidth
  - ✓ EX-SDI 3G - 270Mbps bandwidth
  - ✓ EX-SDI 3.0 4K - 270Mbps bandwidth
- Supports multi formats
  - ✓ 720p 24/25/30/50/60
  - ✓ 1080p 24/25/30/50/60
  - ✓ 1080i 50/60
  - ✓ 1440p 25/30
  - ✓ 2160p 25/30
  - ✓ 1/1.001 Fractional FPS
- Long reach application
- CRC, Line no. correction
- Input auto detection
- UCC(Upstream Communication Cannel)
- I2C Host interface

Outputs

- VD port output 2ch
  - ✓ VD A 2ch-mux output port
  - ✓ VD B bi-direction port
  - ✓ BT.656(8bit) * 2ch
  - ✓ BT.1120(16bit) * 1ch (4K only)
- MIPI-CSI2
  - ✓ Maximum data rate 1188Mbps / Lane
  - ✓ Data Lane 2/4 Lane
  - ✓ Data format YUV8

Power Management

- 1.8V / 3.3V I/O Power
- 1.2V Analog Power
- 1.2V Core Power

Operating Frequency

- Max. 148.5MHz

Operating Ambient Temperature

- -40°C ~ 85°C

Package

- 68QFN 8mm x 8m

2. Pin Diagram

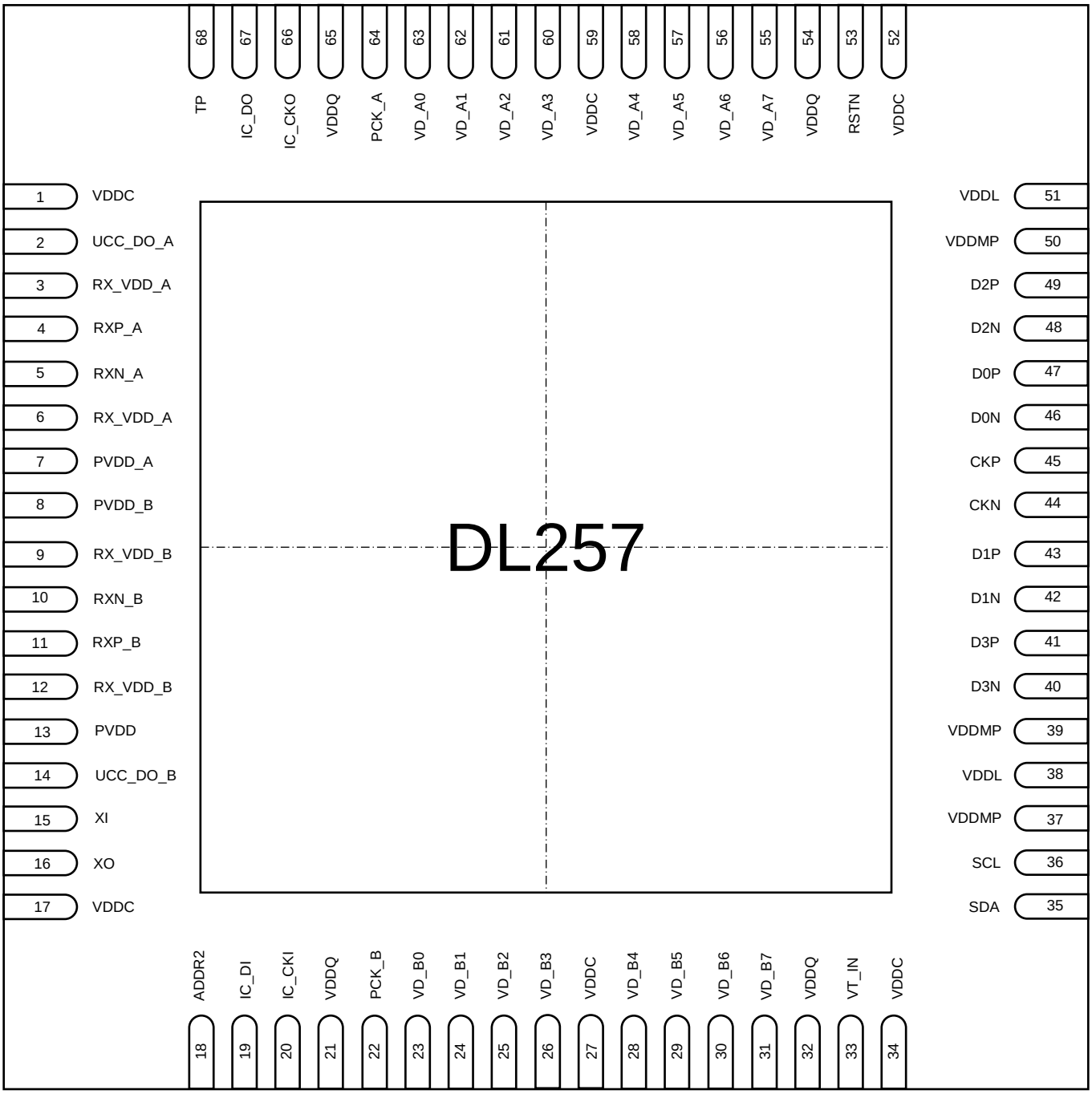


Figure 2-1. DL257 Pin Diagram (Top View)

3. I/O Information

3.1 Pin Description

No.		DL257	I/O	Function	
				Primary	Secondary
LEFT	1	VDDC	P	Core Power 1.2[V]	
	2	UCC_DO_A	I/O	UCC Ch. A output	I2C Address 0
	3	RX_VDD_A	P	RXPHY A Power 1.2[V]	
	4	RXP_A	I	SDI serial data Ch. A positive input	
	5	RXN_A	I	SDI serial data Ch. A negative input	
	6	RX_VDD_A	P	RXPHY A Power 1.2[V]	
	7	PVDD_A	P	RXPHY A PLL Power 1.2[V]	
	8	PVDD_B	P	RXPHY B PLL Power 1.2[V]	
	9	RX_VDD_B	P	RXPHY B Power 1.2[V]	
	10	RXN_B	I	SDI serial data Ch. B negative input	
	11	RXP_B	I	SDI serial data Ch. B positive input	
	12	RX_VDD_B	P	RXPHY B Power 1.2[V]	
	13	PVDD	P	PLL Power 1.2[V]	
	14	UCC_DO_B	I/O	UCC Ch. B output	I2C Address 1
	15	XI	I	System Crystal Clock	
	16	XO	O	System Crystal Clock	
	17	VDDC	P	Core Power 1.2[V]	
BOTTOM	18	ADDR2	I	I2C Address 2	
	19	IC_DI	I	ICIO Data input	
	20	IC_CKI	I	ICIO Data Clock input	
	21	VDDQ	P	IO Power 1.8[V] / 3.3[V]	
	22	PCK_B	I/O	Video Data Clock B input/output	
	23	VD_B0	I/O	Video Data B 0 input/output	
	24	VD_B1	I/O	Video Data B 1 input/output	
	25	VD_B2	I/O	Video Data B 2 input/output	
	26	VD_B3	I/O	Video Data B 3 input/output	
	28	VD_B4	I/O	Video Data B 4 input/output	
	29	VD_B5	I/O	Video Data B 5 input/output	
	30	VD_B6	I/O	Video Data B 6 input/output	
	31	VD_B7	I/O	Video Data B 7 input/output	
	32	VDDQ	P	IO Power 1.8[V] / 3.3[V]	
	33	VT_IN	I/O	Virtual wire Data Input	
	34	VDDC	P	Core Power 1.2[V]	
	35	SDA	I/O	I2C Data	

	36	SCL	I	I2C Clock
RIGHT	37	VDDMP	P	MIPI DPHY Power 1.2[V]
	38	VDDL	P	MIPI Logic Power 1.2[V]
	39	VDDMP	P	MIPI DPHY Power 1.2[V]
	40	D3N	O	MIPI 3 Negative Data
	41	D3P	O	MIPI 3 Positive Data
	42	D1N	O	MIPI 1 Negative Data
	43	D1P	O	MIPI 1 Positive Data
	44	CKN	O	MIPI Negative Clock
	45	CKP	O	MIPI Positive Clock
	46	D0N	O	MIPI 0 Negative Data
	47	D0P	O	MIPI 0 Positive Data
	48	D2N	O	MIPI 2 Negative Data
	49	D2P	O	MIPI 2 Positive Data
	50	VDDMP	P	MIPI DPHY Power 1.2[V]
	51	VDDL	P	MIPI Logic Power 1.2[V]
TOP	52	VDDC	P	Core Power 1.2[V]
	53	RSTN	I	System Reset
	54	VDDQ	P	IO Power 1.8[V] / 3.3[V]
	55	VD_A7	O	Video Data A 7 output
	56	VD_A6	O	Video Data A 6 output
	57	VD_A5	O	Video Data A 5 output
	58	VD_A4	O	Video Data A 4 output
	59	VDDC	P	Core Power 1.2[V]
	60	VD_A3	O	Video Data A 3 output
	61	VD_A2	O	Video Data A 2 output
	62	VD_A1	O	Video Data A 1 output
	63	VD_A0	O	Video Data A 0 output
	64	PCK_A	O	Video Data Clock A output
	65	VDDQ	P	IO Power 1.8[V] / 3.3[V]
	66	IC_CKO	O	ICIO Data Clock output
	67	IC_DO	O	ICIO Data output
	68	TP	I	Test Pin

Table 3-1. Pin Description

3.2 Power Information

Power Name	I/O	Related I/O	Voltage
RX_VDD_A	P	RXP_A, RXN_A	1.2[V]
RX_VDD_B	P	RXP_B, RXN_B	1.2[V]
VDDMP	P	CKP, CKN, D0P, D0N, D1P, D1N, D2P, D2N, D3P, D3N	1.2[V]
VDDQ	P	PCK_A, PCK_B, VD_A0~7, VD_B0~7, IC_CKI, IC_CKO, IC_DI, IC_DO, VT_IN	1.8/3.3[V]

Table 3-2. Power Information

4. Block Diagram

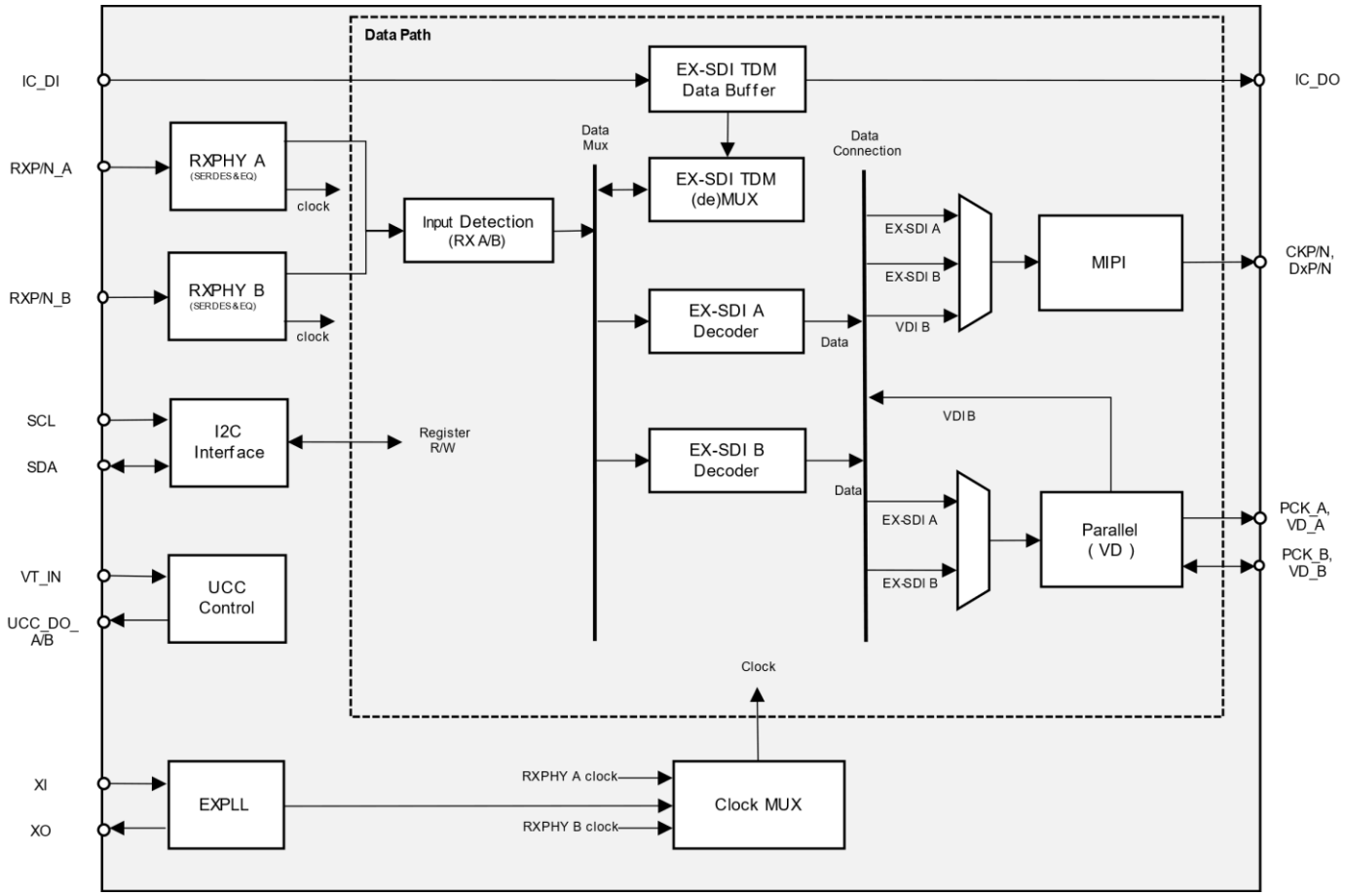


Figure 4-1. Block diagram

The DL257 consists of Analog SerDes part and Digital part. Analog parts have adaptive equalizers, clock data recovery and PLL. Digital parts have descrambler, TRS searcher, word align, EX-SDI decoder, EX-SDI TDM demuxer and MIPI-CSI2. For special function, UCC modulator is integrated for making adjustable frequency-modulation applicable to an external UCC filter circuit.

5. VD port

DL257 VD(Video Data) port is a parallel data bus for SDI inputs or outputs. It composes streams following the SMPTE292m standard. It supports BT1120 20bit or 10bit input/output and DDR clock operation modes. The BT1120 format is showed below. DL257 supports operation range of input/outputs up to 16bit 148.5MHz DDR(4K@30p).

Data Stream Y

Y' 1278	Y' 1279	EAV (3FFh)	EAV (000h)	EAV (000h)	EAV (XYZ)	LN0	LN1	CRC0	CRC1	Optional ancillary data space	SAV(3FFh)	SAV(000h)	SAV(000h)	SAV(XYZ)	Y' 0	Y' 1	Y' 2	Y' 3

Data Stream C

C'_B 639	C'_R 639	EAV (3FFh)	EAV (000h)	EAV (000h)	EAV (XYZ)	LN0	LN1	CRC0	CRC1	Optional ancillary data space	SAV(3FFh)	SAV(000h)	SAV(000h)	SAV(XYZ)	C'_B 0	C'_R 0	C'_B 1	C'_R 1

Figure 5-1. BT1120 20bit data stream

Data Stream Y/C

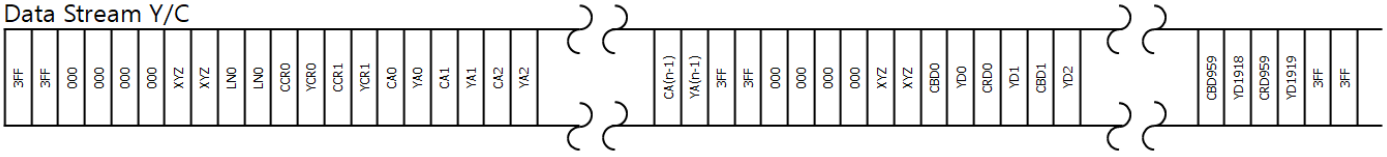


Figure 5-2. BT1120 10bit multiplexed data stream

VD port supported output mode is as follows

- Single rate clock 148.5MHz, YC data 8bit
- Dual rate clock 148.5MHz, YC data 8bit
- Dual rate clock 148.5MHz, Y data 8bit, C data 8bit

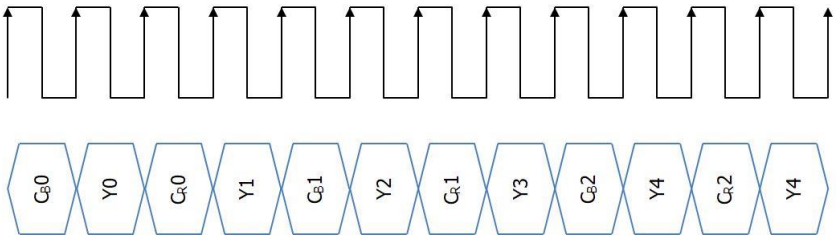


Figure 5-4. Single rate clock 148.5MHz, YC data 10bit

The above waveform is a 1080p30 Multiplexed BT1120 waveform.

- 1.485 Gbps, 148.5 MHz, 8 bit

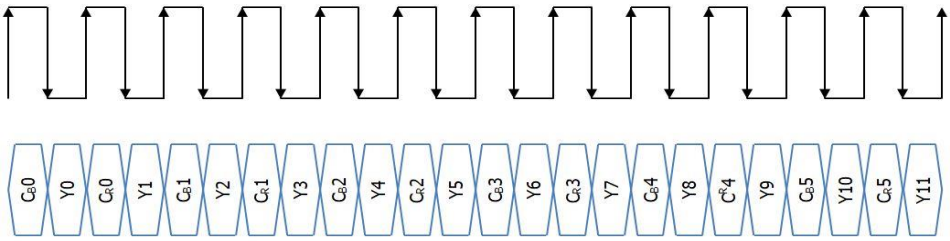


Figure 5-6. Dual rate clock 148.5MHz, YC data 10bit

The upper waveform is a multiplexed BT1120 waveform of 1080p30 * 2ch-mux.

- 2.97Gbps, 148.5MHz DDR, 8bit

6. MIPI TX Specification

- D-PHY Version 1.1 7-Nov-2011
- HS Speed 90 ~ 1188Mbps
- Support 2/4 Data Lane
- Forward (Unidirectional) High-speed only (LPDT/ULPS not support)
- HS differential swing 200mV, HS common level 200mV
- YUV422 8-bit data type supported

Data Type	Description
0x00	Frame Start Code
0x01	Frame End Code
0x02	Line Start Code (Optional)
0x03	Line End Code (Optional)
0x04 to 0x07	Reserved

Figure 6-1. Synchronization Short Packet Data Type Codes

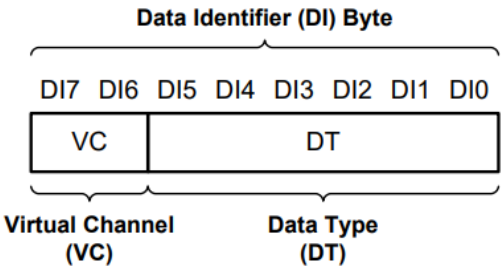


Figure 6-2. Data Identifier Byte

Data Type	Description
0x18	YUV420 8-bit
0x19	YUV420 10-bit
0x1A	Legacy YUV420 8-bit
0x1B	Reserved
0x1C	YUV420 8-bit (Chroma Shifted Pixel Sampling)
0x1D	YUV420 10-bit (Chroma Shifted Pixel Sampling)
0x1E	YUV422 8-bit
0x1F	YUV422 10-bit

Figure 6-3. YUV Image Data Types

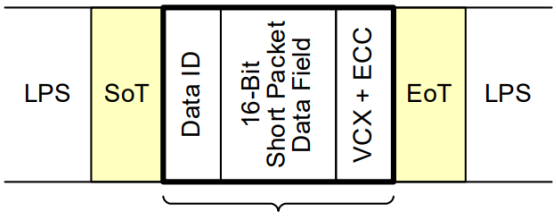


Figure 6-4. Short Packet Structure for D-PHY Physical Layer Option

8-bit DATA IDENTIFIER (DI):
Contains the 2-bit Virtual Channel (VC) and the 6-bit Data Type (DT) Information.
VC (bits 7:6) is the least significant two bits of the 4-bit Virtual Channel Identifier for the D-PHY physical layer option. DT (bits 5:0) denotes the format/content of the Application Specific Payload Data. Used by the application specific layer.

16-bit WORD COUNT (WC):
The receiver reads the next WC data words independent of their values. The receiver is NOT looking for any embedded sync sequences within the payload data. The receiver uses the WC value to determine the end of the Packet Payload.

6-bit Error Correction Code (ECC) + 2-bit Virtual Channel Extension (VCX):
ECC (bits 5:0) enables 1-bit errors within the packet header to be corrected and 2-bit errors to be detected. VCX (bits 7:6) is the most significant two bits of the 4-bit Virtual Channel Identifier for the D-PHY physical layer option.

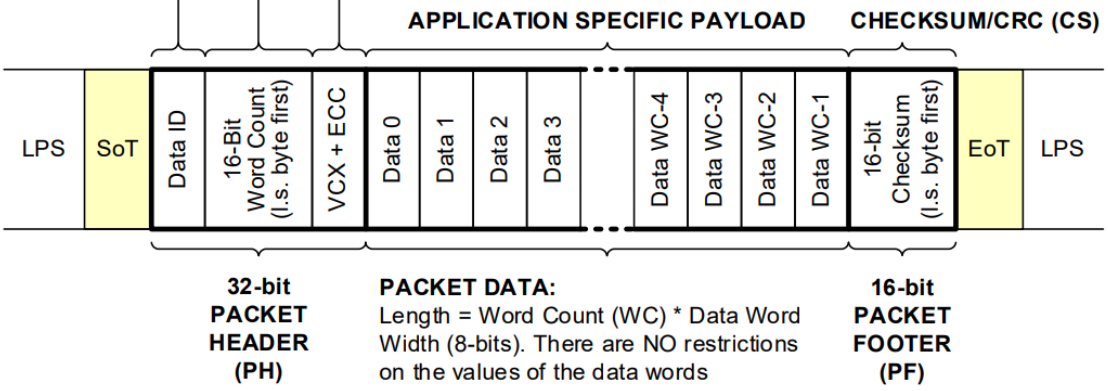


Figure 6-5. Long Packet Structure for D-PHY Physical Layer Option

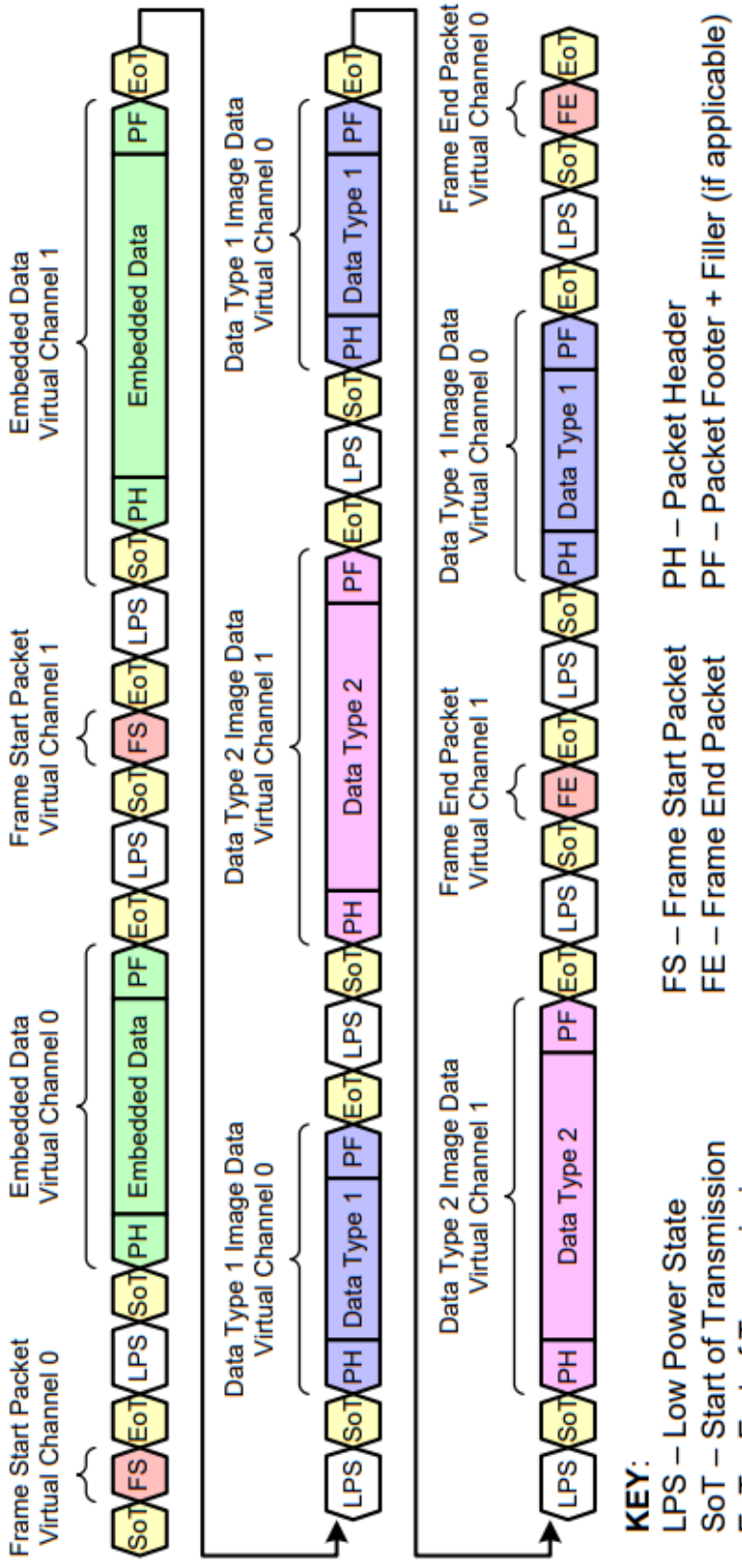


Figure 6-6. Interleaved Data Transmission using Virtual Channels

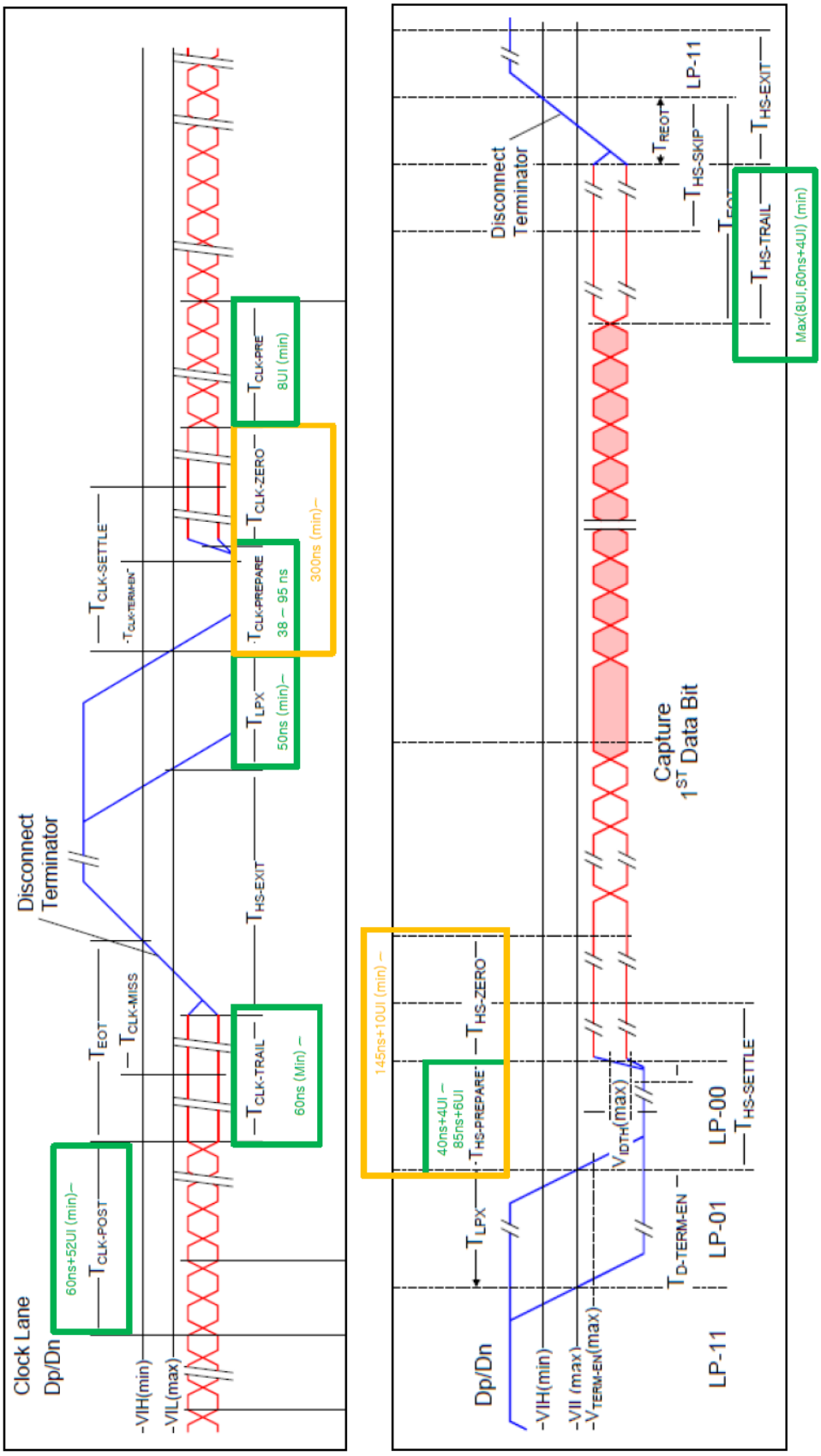


Figure 6-7. MIPI TX operation TX signal Timing

6. Electrical Characteristics

7.1 Absolute Maximum Ratings

(I/O Power: 1.8V / 3.3V)

Symbol	Parameter	Rating			Unit
		Min.	Typ.	Max.	
VDDC	DC Internal Voltage	1.08	1.2	1.32	V
VIN	DC Input Voltage(1.8V)	1.62	1.8	1.98	V
	DC Input Voltage(3.3V)	2.97	3.3	3.63	V
VOUT	DC Output Voltage(1.8V)	1.62	1.8	1.98	V
	DC Output Voltage(3.3V)	2.97	3.3	3.63	V
Latch	Latch-up Current	±100			mA

Table 7-1. Absolute Maximum Ratings

7.2 Recommended Operating Conditions

Symbol	Parameter	Rating	Unit
VDDC	DC Internal Voltage	1.2V±0.12	V
VIN	DC Input Voltage(1.8V)	1.8V±0.18	V
	DC Input Voltage(3.3V)	3.3V±0.33	V
VOUT	DC Output Voltage(1.8V)	1.8V±0.18	V
	DC Output Voltage(3.3V)	3.3V±0.33	V
TOPR	Operating Ambient Temperature	0 to 70	℃
TSTG	Storage Temperature	-40 ~ 125	℃

Table 7-2. Recommended Operation Conditions

7.3 Static Characteristics

	Level			Unit	Note
	Pin	Target	Ref.		
Human Body Model	All	±2,000 ↑		V	
Charged Device Model	All	±500 ↑		V	

Table 7-3. Static Characteristics

7.4 DC Electrical Characteristics

1) DC Electrical Characteristics

Item		Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	Analog	RX_VDD_A	RX_{VDDA}		1.08	1.2	1.32	V
		RX_VDD_B	RX_{VDDB}		1.08	1.2	1.32	V
		PVDD_A	PV_{DDA}		1.08	1.2	1.32	V
		PVDD_B	PV_{DDB}		1.08	1.2	1.32	V
		PVDD	PV_{DD}		1.08	1.2	1.32	V
		VDDMP	V_{DDMP}		1.08	1.2	1.32	V
		VDDL	V_{DDL}		1.08	1.2	1.32	V
	Digital	VDDC	V_{DDC}		1.08	1.2	1.32	V
		VDDQ	V_{DDQ}		1.62/2.97	1.8/3.3	1.98/3.63	V
Digital input voltage		RSTN, XI, TP, VT_IN, VD_B, IC_DI, IC_CKI	V_{IH}		0.7 VDDQ		4	V
			V_{IL}		-0.3		0.3 VDDQ	V
Digital output voltage		UCC_DO_A, UCC_DO_B, PCK_A, PCK_B, VD_A, VD_B, IC_DO, IC_CKO	V_{OH}		VDDQ-0.2			V
			V_{OL}				0.2	V
Serial input Voltage (Common)		RXP_A, RXN_A, RXP_B, RXN_B	V_{CMI}				1.2	V

Table 7-4. DC Electrical Characteristics

2) MIPI TX DC Electrical Characteristics

Parameter	Symbol	Min.	Nom.	Max.	Units
HS transmit static common mode voltage	V_{CMTX}	150	200	250	mV
V_{CMTX} mismatch when output is Differential-1 or Differential-0	$\|V_{CMTX(1,0)}\|$	-	-	5	mV
HS transmit differential voltage	$\|V_{OD}\|$	140	200	270	mV
V_{OD} mismatch when output is Differential-1 or Differential-0	$\|\Delta V_{OD}\|$	-	-	14	mV
HS Output high voltage	V_{OHHS}	-	-	360	mV

Table 7-5. MIPI TX DC Electrical Characteristics

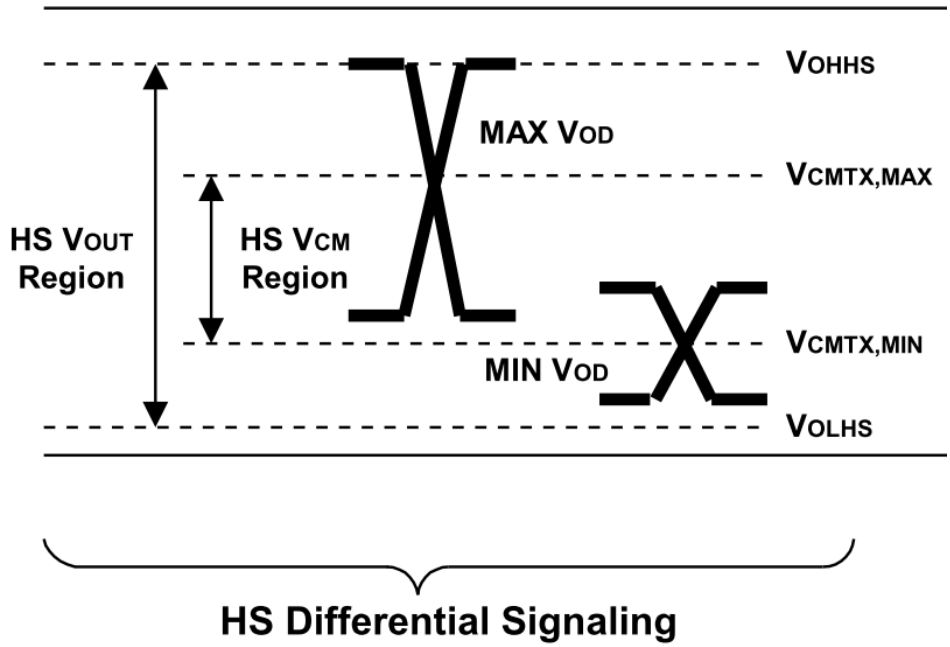


Figure 7-1. MIPI DPHY Signal Level

7.5 AC Electrical Characteristics

1) Main reference clock

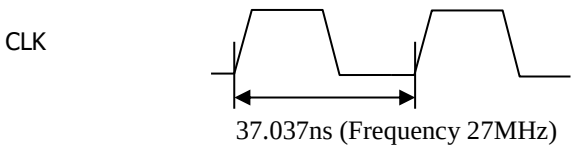


Figure 7-2. main clock description

2) Video output characteristics

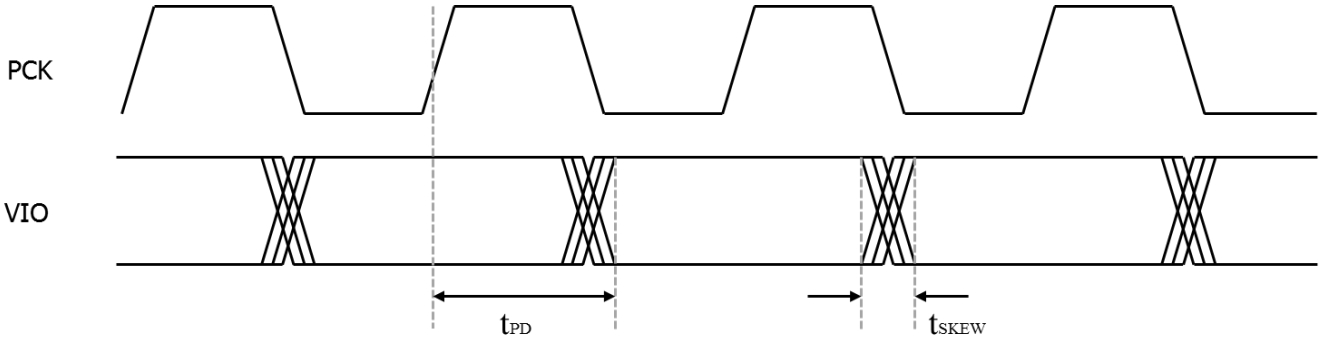


Figure 7-3. VD data output timing diagram

Interface	Symbol	Definition	Min.		Max.		Unit
			VD A	VD B	VD A	VD B	
2M30p 8bit, 148.5Mbps	tPD	PCLK to Data	5.920	5.636	3.393	3.546	ns
	tSKEW	Skew	0.082	0.078	0.245	0.256	ns
4M30p 8bit, 297Mbps	tPD	PCLK to Data	1.423	1.285	0.323	0.332	ns
	tSKEW	Skew	0.097	0.092	0.245	0.256	ns
8M30p 16bit@297Mbps	tPD	PCLK to Data	1.448		0.321		ns
	tSKEW	Skew	0.155		0.259		ns

Table 7-6. VD data output timing value

3) MIPI TX AC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Common-level variations above 450MHz	$\Delta V_{CMTX(HF)}$	-	-	15	mV_{RMS}
Common-level variations between 50 - 450MHz	$\Delta V_{CMTX(LF)}$	-	-	25	mV_{PEAK}
20% - 80% rise time and fall time	tR and tF	-	-	0.35	UI
		100	-	-	ps

Table 7-7. MIPI TX AC Characteristics

4) MIPI TX Clock Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Data to Clock Skew	$T_{SKEW[TX]}$	-0.15		0.15	UI_{INST}
		-0.2		0.2	UI_{INST}

Table 7-8. MIPI TX Clock Characteristics

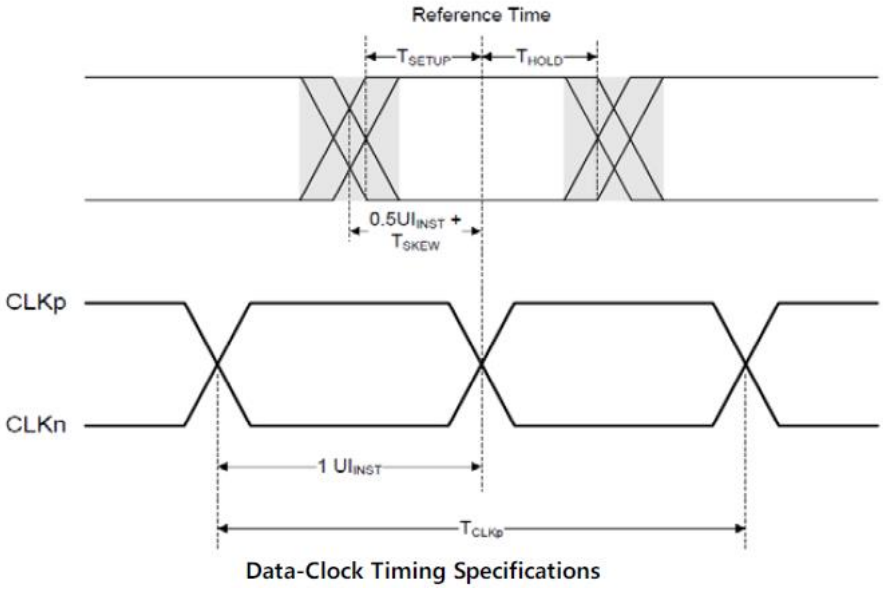


Figure 7-4. MIPI Clock Timing Specifications

7. Power on Sequence

8.1 Power, Reset and Clock

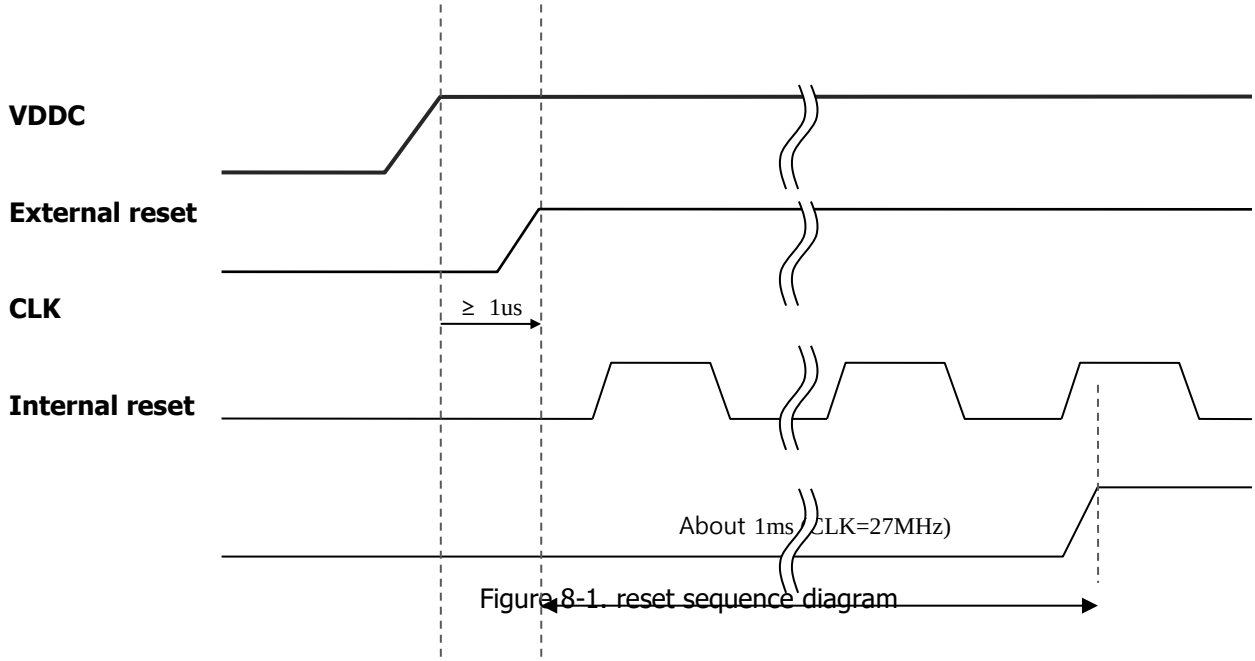


Figure 8-1. reset sequence diagram

After power on, and when external reset is "High", CLK comes in and internal reset will be "high" after 1 ms (CLK at 27 MHz standard). All processes will work when the internal reset is high.

8. Power Consumption

	Input	Output	VDDQ (mA)	VDDC (mA)	PVDD (mA)	RX_VDD_A/B (mA)	PVDD_A/B (mA)	VDDMP (mA)	VDDL (mA)	Total (mW)
			3.3V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	
Case1	CH A, 2M30p EX-SDI v2.0	MIPI 4lane 594MHz 2M30p * 2ch	-	49.4	2.9	25.3	3.6	7.5	22.5	167.5
	CH B, 2M30p EX-SDI v2.0					24.8	3.6			
Case2	CH A, 2M60p EX-SDI v2.0	MIPI 4lane 1188MHz 2M60p * 2ch	-	82.2	2.9	25.3	3.6	12.6	29.7	221.5
	CH B, 2M60p EX-SDI v2.0					24.8	3.6			
Case3	-	MIPI 4lane 1188MHz 2M30p * 4ch Test pattern	-	18.4	2.9	-	-	12.1	29.3	75.2
Case3	CH A, 8M30p EX-SDI v3.0	MIPI 4lane 1188MHz 8M30p	-	84.6	2.9	26.0	3.7	10.4	30.1	189.2
Case4	CH A, 2M30p EX-SDI v2.0	VD A 8bit 148.5Mbps	IOPW0 94.6 IOPW3 112.2	50.9	2.9	25.3	3.6	-	-	445.5
	CH B, 2M30p EX-SDI v2.0	VD B 8bit 148.5Mbps				24.8	3.6			
Case5	CH A, 8M30p EX-SDI v3.0	VD_A/B 297Mbps 8M30p	IOPW0 81.8 IOPW3 96.8	51.6	2.9	26	3.7	-	-	371.0

9. Table 9-1. Power Consumption

Note)

It is not all function operation.

It is measurement value.

10. Video Output Interface

10.1 Interface Overview

The following table lists available interfaces between DL257s and SoC according to input sources and output types.

Interface #	Input Source	Output Type	Output Ch. #	Clock rate	Data rate	Interleave
1	2M30p * 4	DVP	4	148.5MHz	148.5Mbps (SDR)	none
	2M60p * 4				297Mbps (DDR)	
2	2M30p * 4		2	148.5MHz	297Mbps (DDR)	2ch
3	4K30p*2		4	148.5MHz	297Mbps (DDR)	none
4	2M30p * 4	MIPI	2	594Mbps/lane		2ch Virtual ID
	2M60p * 4			1188Mbps/lane		2ch Virtual ID
5	4K30p*2		2	1188Mbps/lane		2ch Virtual ID
6	2M30p * 4		1	1188Mbps/lane		4ch Virtual ID

Table 10-1. Interface Overview (Based on two DL257s)

10.2 Interface #1

This interface supports the following features

- 2M30p/60p * 4 channels
- EX-SDI
- BT.656/BT.1120 base format
- 8bit base output via Parallel bus
- 148.5Mbps single data rate with 148.5MHz in 2M30p
- 297Mbps dual data rate with 148.5MHz in 2M60p

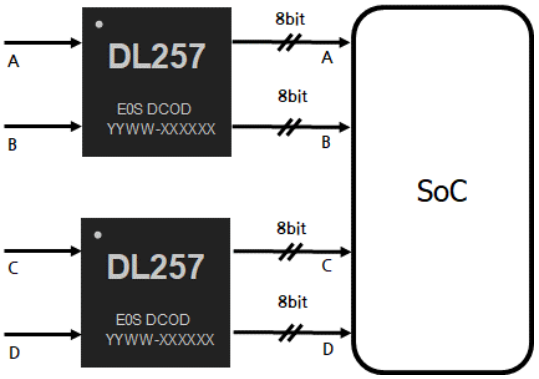


Figure 10-2. Interface #1

10.3 Interface #2

This interface supports the following features

- 2M30p * 4 channels
- EX-SDI
- BT.656/BT.1120 base format
- 8bit base output via Parallel bus
- 297Mbps dual data rate with 148.5MHz (2ch byte interleave of 4ch source)

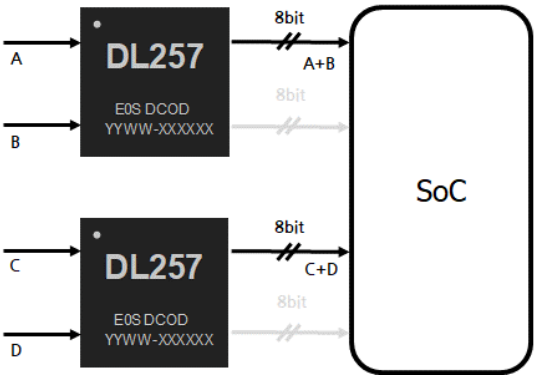


Figure 10-2. Interface #2

10.4 Interface #3

This interface supports the following features

- 8M30p(4K30p) * 2 channels
- EX-SDI
- BT.1120 base format
- 16bit base output via Parallel bus
- 297Mbps dual data rate with 148.5MHz

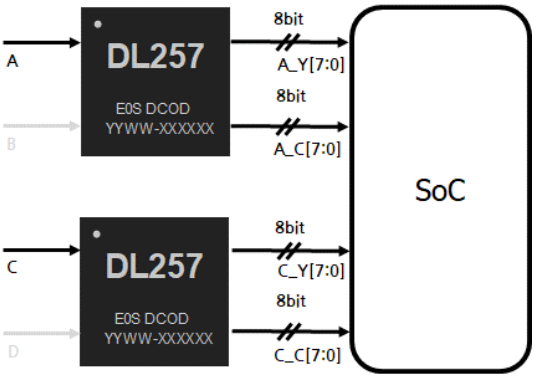


Figure 10-3. Interface #3

10.5 Interface #4

This interface supports the following features

- 2M30p/60p * 4 channels
- EX-SDI
- MIPI CSI2 outputs (2 Lane/4 Lane)
- 8bit base output via MIPI bus
- 594Mbps/lane(4 Lane) / 1188Mbps/lane(2 Lane)

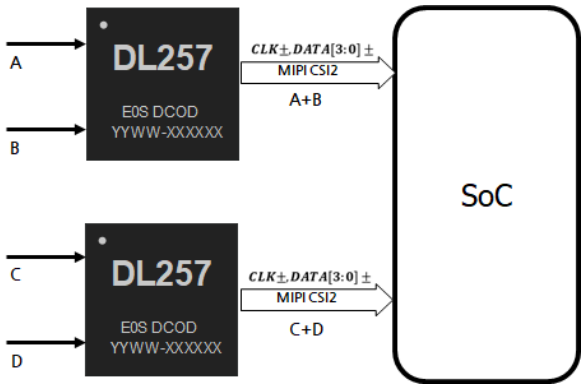


Figure 10-5. Interface #5

10.6 Interface #5

This interface supports the following features

- 8M30p(4K30p) * 2 channels
- EX-SDI
- MIPI CSI2 outputs (4 Lane)
- 8bit base output via MIPI bus
- 1188Mbps /lane(4 Lane)

Figure 10-6. Interface #6

10.7 Interface #6

This interface supports the following features

- 2M30p * 4 channels
- EX-SDI
- MIPI CSI2 outputs (4 Lane)
- 8bit base output via MIPI bus
- 1188Mbps /lane(4 Lane)

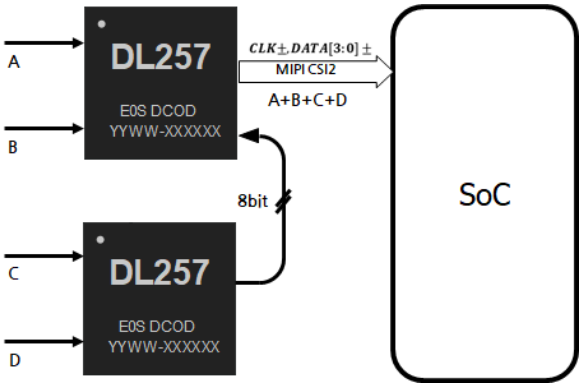


Figure 10-7. Interface #7

11. Functional Overview

11.1 EX-SDI

Generally achievable distance is in inverse proportion to transmission rate. With RG59 cable, transmission distance is approximately 330m in 270Mbps, 160m in 1.485Gbps and 100m in 2.98Gbps. EX-SDI V1.0 supports only 270Mbps–transmission with 20% image compression. This makes HD-SDI (1.485Gbsp data rate) go over 300m and go over low-end cable.

EX-SDI V2.0 supports not only 270Mbps but also 135Mbps, transmission distance is much longer than V1.0. The expected reach is over 500m with RG59 cable. Furthermore, it's helpful to reduce difficulties to use low-end cable such UTP and 3C-2V. EX-SDI V2.1 supports 3G/4M video resolution based on 270Mbps bandwidth and supports 4K video resolution based on 1.5Gbps bandwidth. Also compatible with EX-SDI V2.0 and below.

Moreover, since EX-SDI V3.0 supports 4K video resolution based on 270Mbps bandwidth. And also compatible with EX-SDI V2.1 and below.

EX-SDI is a visually lossless codec based on JPEG standard. Its processing is simple as shown below figure. It is composed of compress codec, domain conversion and codec rate controller. Codec controller controls compression rate while studying optimal point of buffer. Optimal point is where total amount of compressed data is as much as empty buffer size by outputting data in buffer.

Therefore, image quality relies on this controller. The PSNR is normally 40dB and more in normal source.

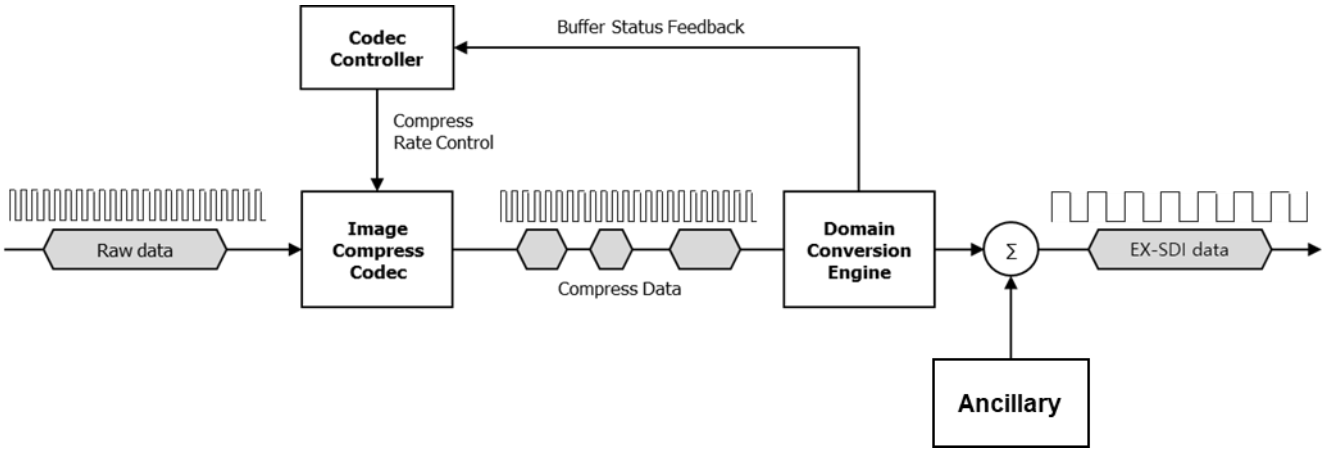


Figure 10-1. EX-SDI compress sequence

EX-SDI	V1.0	V2.0	V2.1	V3.0	Channel Coding	Polarity Free	UCC/ PoC
135Mbps		720p30	←	←	8b/10b	X	O
		720p60	←	←			
		1080p30	←	←			
135Mbps+			720p30	←	8b/10b	X	O
			720p60	←			
			1080p30	←			
270Mbps	720p30	←	←	←	Scrambled NRZ	O	X
	720p60	←	←	←			
	1080p30	←	←	←			
			1080p60	←	8b/10b	X	O
			1440p30	←			
				2160p30			
				1080p120			
1.5Gbps			2160p30	←	Scrambled NRZ	O	O
				2160p60	8b/10b	X	O
HD-SDI	O	O	X	X			
3G-SDI	O	X	X	X			
Tx device	→	→	→	EN870 EN801S EN801M			
	→	→	EN779				
	→	EN771					
	EN773V						
	EN778						
Rx device	→	→	→	EN351T DL257 DL357			
	→	→	EN332T				
	→	→	EN334S				
	→	EN332					
	→	EN334R					
	EN331						

Table 10-1. EX-SDI generation

<table>
<tr><th>EX-SDI TDM Ver.</th><th>V1.0</th><th>V1.1</th><th>Channel Coding</th><th>Polarity Free</th><th>UCC/ PoC</th></tr>
<tr><td>270Mbps</td><td></td><td>1080p30 4ch</td><td>8b/10b</td><td>X</td><td>O</td></tr>
<tr><td rowspan="4">1.5Gbps</td><td>1080p30 8ch</td><td>←</td><td>8b/10b NRZ</td><td>O</td><td rowspan="4">O</td></tr>
<tr><td></td><td>1080p60 4ch</td><td rowspan="3">8b/10b</td><td rowspan="3">X</td></tr>
<tr><td></td><td>1440p30 4ch</td></tr>
<tr><td></td><td>2160p30 4ch</td></tr>
<tr><td rowspan="2">Tx device</td><td>→</td><td rowspan="2">EN781
EN772
EN781</td><td colspan="3" rowspan="4">P30 covers P29.97 and P25
P60 covers P59.94 and P50
1440P 4Mpix : 2560x1440
2160P 8Mpix 4K : 3840x2176</td></tr>
<tr><td>EN332T</td></tr>
<tr><td rowspan="3">Rx device</td><td>→</td><td rowspan="3">EN351
DL357</td></tr>
<tr><td>EN332T</td></tr>
<tr><td>EN334U</td></tr>
</table>

Table 10-2. EX-SDI TDM generation

11.2 UCC (Upstream Communication Channel)

UCC is a function to control a camera in DVR side over Coax cable remotely. The DL257 has a UCC modulator inside, which can modulate commonly used control signals (UART, Pelco…) with 0.5MHz ~ 10MHz carrier frequency. With an associated UCC filter, modulated data can go upstream to the camera over coax cable while video data is going downstream from the camera.

In addition, it has UART generator in itself. It can make maximum 16byte serial UART data and outputting it to UCC modulator module.

※ Please see UCC guide document for more details)

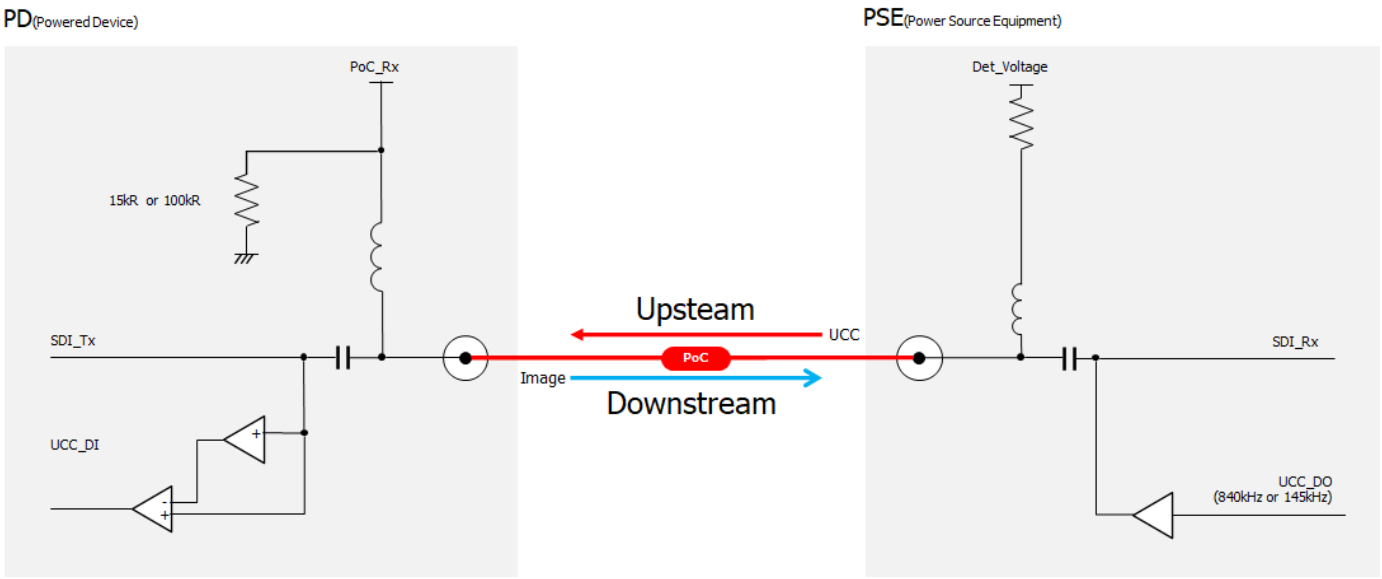


Figure 11-3. UCC & PoC application diagram

11.3 Channel coding

The SDI standard defines scrambled NRZ as a channel coding. Scrambling signal makes it statistically likely to have a low DC content for easier handling and have a greater number of transitions for easier clock recovery without any bit redundancy (Polynomial $G1(X) = X^9 + X^4 + 1$, $G2(X) = X + 1$).

In order to convert available signal from SDI to parallel data, NRZI-to-NRZ and descrambling processing must be applied before main processing.

The traditional scrambling method used in SDI has a few advantages like no redundancy and polarity-free. Although under normal condition the scrambled data has high transition with an even ratio of ones to zeros, some scrambled status meets too challenging conditions for the receiver to reconstruct SDI signal.

For more reliable communication, EX-SDI 2.0 adopted 8B/10B instead of the scrambled NRZ, even though it has 2 bit redundancy. This helps to achieve DC-balance to reduce the risk of data miss-acquisition in CDR of a receiver side.

Mode	Data rate (bps)	Signal Encoding	Polarity free
EX-SDI V1.0	270M	Scrambled NRZ	O
EX-SDI V2.0	135M	8b/10b[1)]	X
EX-SDI 3G/4M/4K	270M	8b/10b[1)]	X

Note[1)]: DL257 is input polarity-switchable, but it's controlled manually.

Table 11-3. EX-SDI signal encoding and Polarity

11.4 Video format detector

The DL257 supports various video formats as well as the defined in SMPTE.

The video detector module identifies the format of the incoming video data, and extracts information as listed below.

- Total horizontal pixel in a line
- Total vertical line in a frame
- Interlace or Progress
- Frame rate (1 or 1000/1001)
- EX-SDI

The above information is updated to the resisters to be accessed by MCU.

11.5 CRC detector and Counting

The CRC is an error-detecting code used in a digital network. EX-SDI has the packet-based CRC calculated every EX-SDI packet. Each packet has a different length and size according to the compressed quantity. The DL257 extracts CRC value from the specific position (i.e. every end of packet in EX-SDI), while it re-generates a new CRC value from incoming data. When the extracted one and the re-generated one is the same, CRC counter keep the previous counter, otherwise when they are different, the counter increases. The CRC is commonly used to check channel integrity to make sure of error free.

11.6 Pattern generator

The DL257 has a flexible video pattern generator that makes up to 4096x2160 format as well as HD format with the associated data clock and TRS. The pattern types can be configured by control registers belonging to each channel. In addition to video, the frequency and amplitude - adjustable Sine wave can be generated for audio test pattern replacing SDI embedded audio.

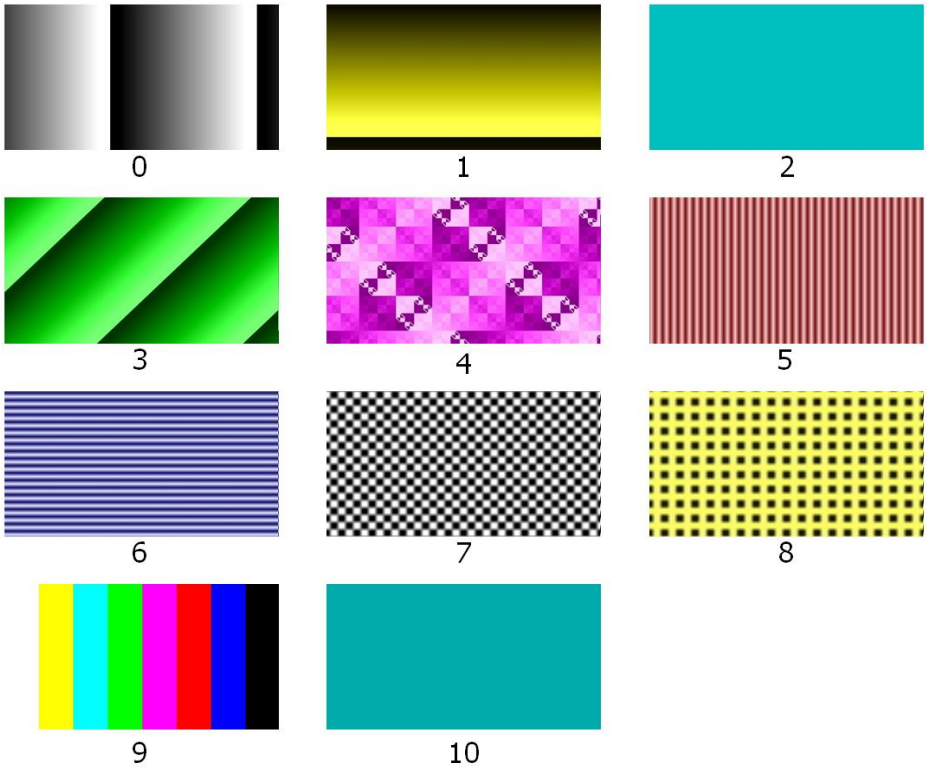


Figure 11-4. Internal test pattern

All Pattern

No.	PGEN_ YPAT[23:16]	PGEN_ CRPAT[15:8]	PGEN_ CBPAT[7:0]	Description
0	0x0	0x80	0x80	Horizontal
1	0x1	0x2c	0x88	Vertical
2	0x2	0x93	0x2c	Flicker
3	0x3	0x3f	0x34	Diagonal
4	0x4	0xc1	0xcc	Lattice
5	0x5	0x6d	0xd4	H High Resolution
6	0x6	0xd4	0x78	V High Resolution
7	0x7	0x80	0x80	Dot High Resolution
8	0x8	0x2c	0x88	Dot High Resolution
9[1)]	0x9	-	-	Color Bar
10	0xa	0x93	0x80	Flat

[1)] **PGEN_FIX_VAL[9] = '0'**

Table 11-4. Inter test pattern register set value

11.7 I2C

The DL257 has I2C capability. Refer to below Figure for I2C sequence. Page Address is '0x0'.

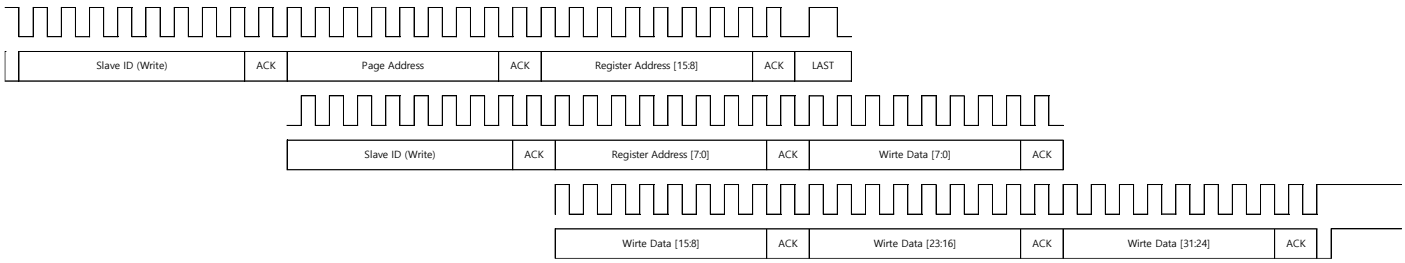


Figure 11-5. I2C Write sequence

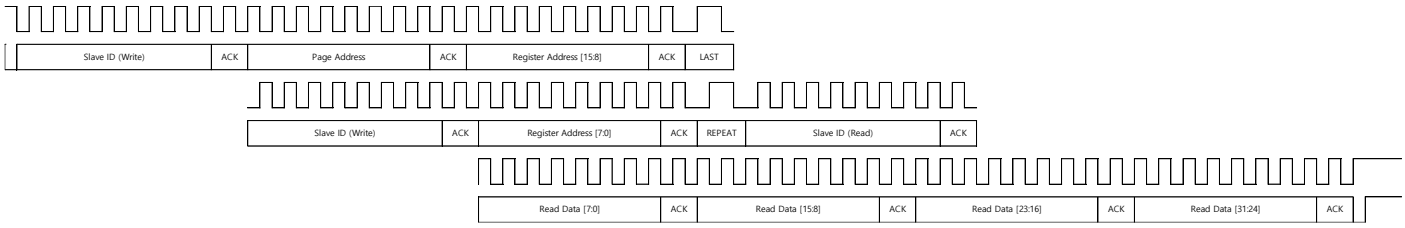


Figure 11-6. I2C Read sequence

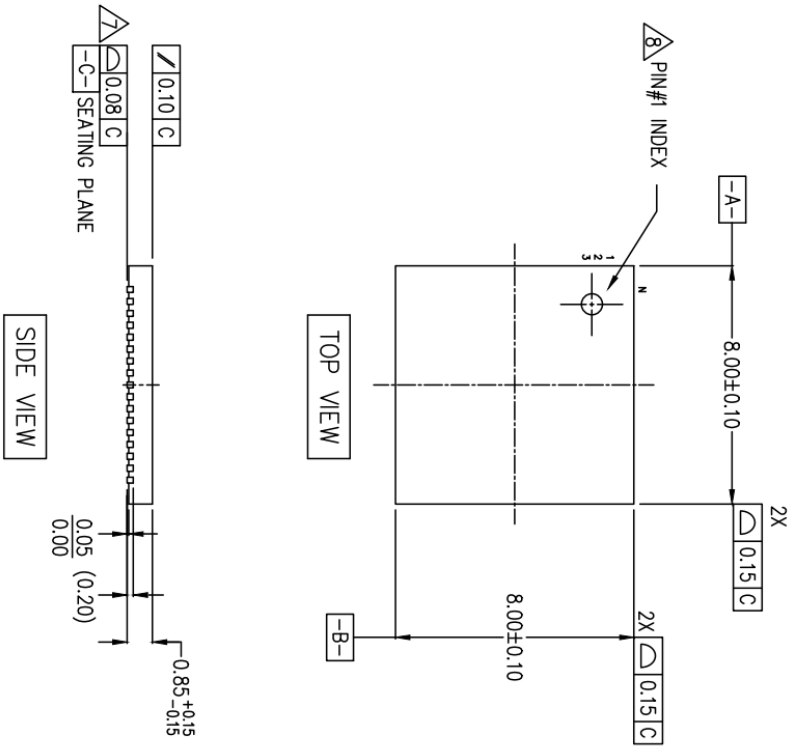
The I2C address is determined by the UCC_DO_A, UCC_DO_B, ADDR2 pins.

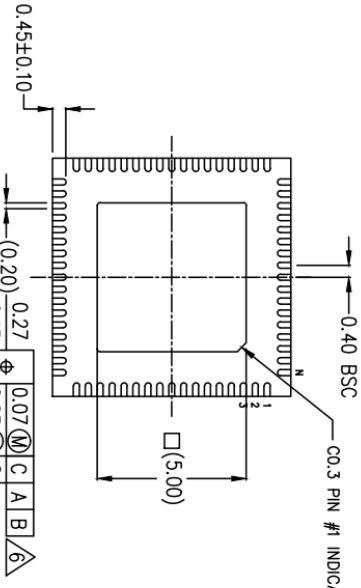
Refer to the table below for I2C address setting.

7	6	5	4	3	2	1	0
1	0	ADDR2	UCC_DO_B	UCC_DO_A	1	0	R/W

Table 11-5. I2C Address setting

12. Package Dimension



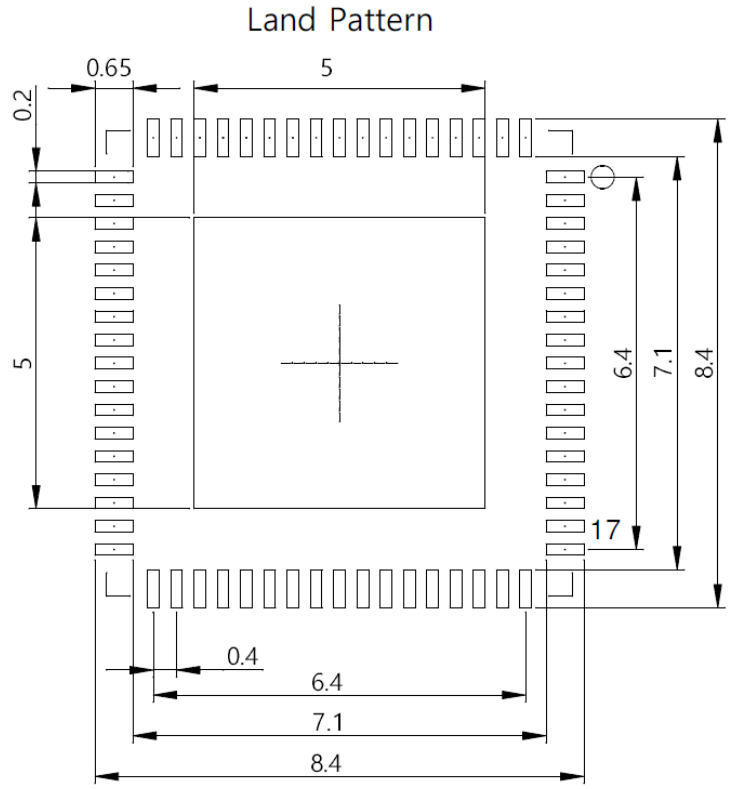


NOTES :

1. PACKAGE DIMENSIONS CONFORM TO JEDEC MO-220.
2. DIMENSIONING AND TOLERANCING CONFORM TO ASEM Y 14.5M - 1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS. ( ) IS REFERENCE.
4. MAXIMUM ALLOWABLE BURR SHALL NOT EXCEED 0.05MM.
5. LEAD NUMBERS START WITH THE #1 AND CONTINUE COUNTCLOCKWISE TO LEAD #68 WHEN VIEWED FROM THE TOP.
6. LEAD WIDTH IS MEASURED BETWEEN 0.15MM AND 0.27MM FROM THE LEAD TIP.
7. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE LEADS.
8. PIN #1 INDEX MUST BE INDICATED BY LASER MARK.

13. Footprint Layout

Example Board Layout



Initial Release	2021-08-18	DWG No.	ENDWG-21081801
Update		Title	
Rev.	0		
Tolerance	.XXX±0.005	Description	VQFN68, 0.4mm pitch, 8x8mm
Unit	mm	Drawing	nhkim
Scale	5:1		